512M Low Power Mobile SDRAM (MSDR)

Revision History
512M AS4C32M16MS-7BCN/AS4C32M16MS-6BIN - 54 ball FBGA PACKAGE
512M AS4C16M32MS-7BCN/AS4C16M32MS-6BIN - 90 ball FBGA PACKAGE

Revision	Details	Date
Rev 1.0	Preliminary datasheet	Jun 2016

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Features

- 4 banks x 8Mbit x 16 organization
- 4 banks x 4Mbit x 32 organization
- High speed data transfer rates up to 166 MHz
- Full Synchronous Dynamic RAM, with all signals referenced to clock rising edge
- Single Pulsed $\overline{RAS}$ Interface
- Data Mask for Read/Write Control
- Four Banks controlled by BA0 & BA1
- Programmable $\overline{CAS}$ Latency: 2, 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length:
  1, 2, 4, 8, Full page for Sequential Type
  1, 2, 4, 8 for Interleave Type
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Random Column Address every CLK (1-N Rule)
- Power Down Mode and Clock Suspend Mode
- Auto Refresh and Self Refresh
- Refresh Interval:
  8192 cycles/64 ms
- Available in 54-ball (32M x16) and 90-ball (16M x32)FBGA
- VDD=1.8V, VDDQ=1.8V
- LVTTL Interface
- Drive Strength (DS) Option: Full, 1/2, 1/4 and 3/4
- Auto Temperature Compensated Self Refresh (Auto TCSR)
- Partial Array Self Refresh (PASR) option: Full, 1/2, 1/4, 1/8 and 1/16
- Deep Power Down (DPD) mode
- Programmable Power Reduction Feature by patial array activation during Self-Refresh
- Operating Temperature Range
  Commercial (-25°C to 85°C)
  Industrial (-40°C to +85°C)

Table 1. Key Specifications

AS4C32M16MS/AS4C16M32MS		-6/7
tCK(3)	Clock Cycle time(min.)	6/7.5 ns
tAC(3)	Access time from CLK (max.)	5/5.4 ns
tRAS	Row Active time(min.)	42/45 ns
tRC	Row Cycle time(min.)	60/67.5 ns

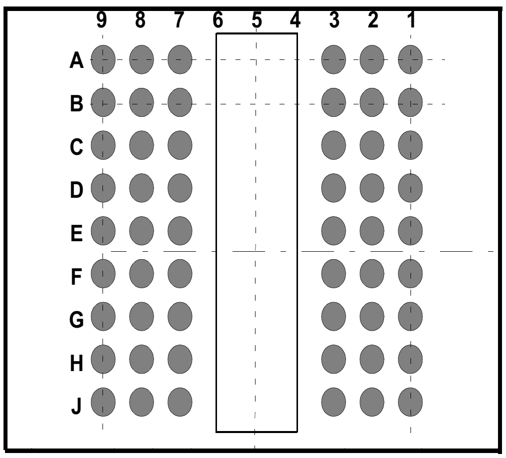
Table 2. Ordering Information

Part Number	Org	Temperature	MaxClock (MHz)	Package
AS4C32M16MS-7BCN	32Mx16	Commercial -25°C to +85°C	133	54-ball FBGA
AS4C32M16MS-6BIN	32Mx16	Industrial -40°C to +85°C	166	54-ball FBGA
AS4C16M32MS-7BCN	16Mx32	Commercial -25°C to +85°C	133	90-ball FBGA
AS4C16M32MS-6BIN	16Mx32	Industrial -40°C to +85°C	166	90-ball FBGA

512Mb Mobile SDRAM Addressing

Configuration	**32MX16**	**16MX32**	**16MX32 (Reduced page size)**
# of Bank	4	4	4
Bank Address	BA0 ~ BA1	BA0 ~ BA1	BA0 ~ BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A12	A0 ~ A12	A0 ~ A13
Column Address	A0 ~ A9	A0 ~ A8	A0 ~ A7

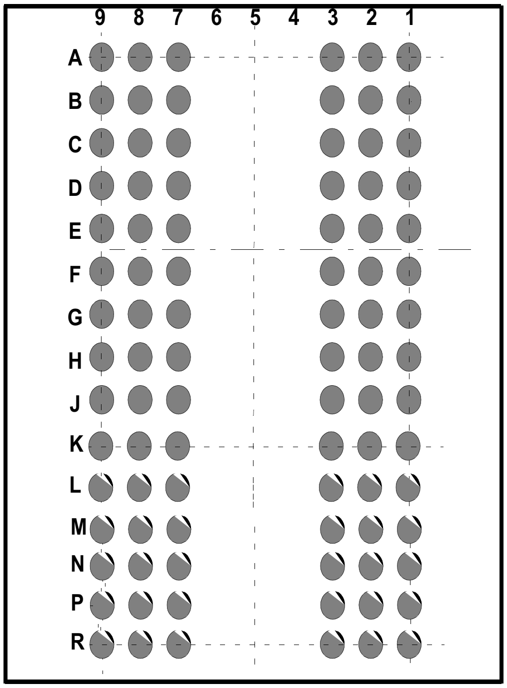
54 Pin (X16) BGA PIN CONFIGURATION
Top View



54Ball(6X9)CSP						
	1	2	3	7	8	9
A	VSS	DQ15	VSSQ	VDDQ	DQ0	VDD
B	DQ14	DQ13	VDDQ	VSSQ	DQ2	DQ1
C	DQ12	DQ11	VSSQ	VDDQ	DQ3	DQ3
D	DQ10	DQ9	VDDQ	VSSQ	DQ6	DQ5
E	DQ8	DNU[1]	VSS	VDD	LDQM	DQ7
F	UDQM	CK	CKE	$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	A12	A11	A9	BA0	BA1	$\overline{CS}$
H	A8	A7	A6	A0	A1	A10/AP
J	VSS	A5	A4	A3	A2	VDD

Note 1: The DNU pin must be connected to VSS, VSSQ, or left floating.

90 Pin (X32) BGA PIN CONFIGURATION
Top View



90Ball(6X15)CSP						
	1	2	3	7	8	9
A	DQ26	DQ24	VSS	VDD	DQ23	DQ21
B	DQ28	VDDQ	VSSQ	VDDQ	VSSQ	DQ19
C	VSSQ	DQ27	DQ25	DQ22	DQ20	VDDQ
D	VSSQ	DQ29	DQ30	DQ17	DQ18	VDDQ
E	VDDQ	DQ31	NC	NC	DQ16	VSSQ
F	VSS	DQM3	A3	A2	DQM2	VDD
G	A4	A5	A6	A10/AP	A0	A1
H	A7	A8	A12	A13[1]	BA1	A11
J	CK	CKE	A9	BA0	$\overline{CS}$	$\overline{RAS}$
K	DQM1	DNU[2]	NC	$\overline{CAS}$	$\overline{WE}$	DQM0
L	VDDQ	DQ8	VSS	VDD	DQ7	VSSQ
M	VSSQ	DQ10	DQ9	DQ6	DQ5	VDDQ
N	VSSQ	DQ12	DQ14	DQ1	DQ3	VDDQ
P	DQ11	VDDQ	VSSQ	VDDQ	VSSQ	DQ4
R	DQ13	DQ15	VSS	VDD	DQ0	DQ2

Note 1: A13 is only available for reduced page-size configuration.
Note 2: The DNU pin must be connected to VSS, VSSQ, or left floating.

Description

The AS4C32M16MS / AS4C16M32MS is a four bank Synchronous DRAM organized as 4 banks x 8Mbit x 16 and 4 banks x 4Mbit x 32. The AS4C32M16MS / AS4C16M32MS achieves high speed data transfer rates up to 166 MHz by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleaved fashion allows random access operation to occur at higher rate than is possible with standard DRAMs. A sequential and gapless data rate of up to 166 MHz is possible depending on burst length, $\overline{\text{CAS}}$ latency and speed grade of the device.

Signal Pin Description

Pin	Type	Signal	Polarity	Function
CLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
CKE	Input	Level	Active High	Activates the CLK signal when high and deactivates the CLK signal when low, thereby initiates either the Power Down mode or the Self Refresh mode.
$\overline{\text{CS}}$	Input	Pulse	Active Low	$\overline{\text{CS}}$ enables the command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ $\overline{\text{WE}}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ define the command to be executed by the SDRAM.
A0 - A13	Input	Level	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) and A0-A13 defines the row address (RA0-RA13) for 16Mx32 reduced page size when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) for 32Mx16, A0-A8 defines the column address (CA0-CA8) for 16Mx32 and A0-A7 defines tthe column address (CA0-CA7) for 16Mx32 reduced page size when sampled at the rising clock edge. In addition to the column address, A10(=AP) is used to invoke autoprecharge operation at the end of the burst read or write cycle. If A10 is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If A10 is low, autoprecharge is disabled. During a Precharge command cycle, A10(=AP) is used in conjunction with BA0 and BA1 to control which bank(s) to precharge. If A10 is high, all four banks will BA0 and BA1 are used to define which bank to precharge.
BA0, BA1	Input	Level	—	Selects which bank is to be active.
DQx	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
LDQM UDQM (DM0~3)	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a word mask by allowing input data to be written if it is low but blocks the write operation if DQM is high. If it's high, LDM corresponds to DQ0-DQ7, and UDM corresponds to data on DQ8-DQ15 in 32Mx16. DM0 corresponds to DQ0-DQ7, DM1 corresponds to data on DQ8-DQ15, DM2 corresponds to DQ16-DQ23, and DM3 corresponds to data on DQ24-DQ31 in 16Mx32.
VDD, VSS	Supply			Power and ground for the input buffers and the core logic.
VDDQ VSSQ	Supply	—	—	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	Input	—	—	No connect.

Operation Definition

All of SDRAM operations are defined by states of control signals $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and DQM at the positive edge of the clock. The following list shows the thruth table for the operation commands.

Operation	Device State	CKE n-1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	A0-9, A11,12	A10	BA0 BA1
Row Activate	Idle[3]	H	X	L	L	H	H	X	V	V	V
Read	Active[3]	H	X	L	H	L	H	X	V	L	V
Read w/Autoprecharge	Active[3]	H	X	L	H	L	H	X	V	H	V
Write	Active[3]	H	X	L	H	L	L	X	V	L	V
Write with Autoprecharge	Active[3]	H	X	L	H	L	L	X	V	H	V
Row Precharge	Any	H	X	L	L	H	L	X	X	L	V
Precharge All	Any	H	X	L	L	H	L	X	X	H	X
Mode Register Set	Idle	H	X	L	L	L	L	X	V	V	V
No Operation	Any	H	X	L	H	H	H	X	X	X	X
Device Deselect	Any	H	X	H	X	X	X	X	X	X	X
Auto Refresh	Idle	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry [6]	Idle	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit [6]	Idle (Self Refr.)	L	H	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Entry	Idle Active[4]	H	L	H	X	X	X	X	X	X	X
				L	H	H	X				
Power Down Exit	Any (Power Down)	L	H	H	X	X	X	X	X	X	X
				L	H	H	L				
Data Write/Output Enable	Active	H	X	X	X	X	X	L	X	X	X
Data Write/Output Disable	Active	H	X	X	X	X	X	H	X	X	X
Deep Power Down Entry	Idle	H	L	L	H	H	L	X	X	X	X
Deep Power Down Exit	Deep power-Down	L	H	X	X	X	X	X	X	X	X

Notes:
1. V = Valid , x = Don't Care, L = Low Level, H = High Level
2. CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3. These are state of bank designated by BA0, BA1 signals.
4. Power Down Mode can not entry in the burst cycle.
5. After Deep Power Down mode exit a full new initialization of memory device is mandatory
6. Extended grade does not guarantee self-refresh function

Power On and Initialization

The default power on state of the mode register is supplier specific and may be undefined. The following power on and initialization sequence guarantees the device is preconditioned to each users specific needs. Like a conventional DRAM, the Synchronous DRAM must be powered up and initialized in a pre-defined manner. During power on, all VDD and VDDQ pins must be built up simultaneously to the specified voltage when the input signals are held in the “NOP” state. The CLK signal must be started at the same time. After power on, the device requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100us period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied. After the 100us delay is satisfied by issuing at least one COMMAND INHIBIT or NOP command, a PRECHARGE command must be issued. All banks must then be pre-charged, which places the device in the all banks idle state. Once all banks have been pre-charged, the Mode Register and Extended Mode Register Set Command must be issued to initialize the Mode Register. A minimum of two Auto Refresh cycles (CBR) are also required. These may be done before or after programming the Mode Register. Failure to follow these steps may lead to unpredictable start-up modes.

Programming the Mode Register

The Mode register designates the operation mode at the read or write cycle. This register is divided into 4 fields. A Burst Length Field to set the length of the burst, an Addressing Selection bit to program the column access sequence in a burst cycle (interleaved or sequential), a CAS Latency Field to set the access time at clock cycle and a Operation mode field to differentiate between normal operation (Burst read and burst Write) and a special Burst Read and Single Write mode. The mode set operation must be done before any activate command after the initial power up. Any content of the mode register can be altered by re-executing the mode set command. All banks must be in pre-charged state and CKE must be high at least one clock before the mode set operation. After the mode register is set, a Standby or NOP command is required. Low signals of RAS, CAS, and WE at the positive edge of the clock activate the mode set operation. Address input data at this timing defines parameters to be set as shown in the previous table.

Extended Mode Register

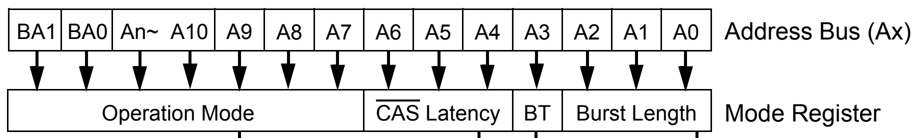
The extended Mode Register controls functions beyond those controlled by the Mode Register. These additional functions are unique to the mobile SDRAM and includes the selection of drive strength (DS). The device has four drive strength options: Full, 12, 1/4 or 3/4. And a Partial-Array Self-Refresh field (PASR). The PASR field is used to specify whether partial bank 1/2, 1/4, 1/8, 1/16 or all banks of the SDRAM array are enabled. Disabled banks will not be refreshed in Self-Refresh mode and written data will be lost. When only bank 0 is selected, it’s possible to partially select only half or more quarter of bank 0. The default setting for DS is full-strength, while PASR is full memory. Both DS and PASR can be set during the initialization sequence and can be modified when the part is idle. Additionally, the device has internal temperature sensor control self refresh cycle automatically. This is the device internal Temperature Compensated Self Refresh (TCSR).

Read and Write Operation

When RAS is low and both CAS and WE are high at the positive edge of the clock, a RAS cycle starts. According to address data, a word line of the selected bank is activated and all of sense amplifiers associated to the wordline are set. A CAS cycle is triggered by setting RAS high and CAS low at a clock timing after a necessary delay, t_{RCD}, from the RAS timing. WE is used to define either a read (WE = H) or a write (WE = L) at this stage.

SDRAM provides a wide variety of fast access modes. In a single CAS cycle, serial data read or write operations are allowed at up to a 166 MHz data rate. The numbers of serial data bits are the burst length programmed at the mode set operation, i.e., one of 1, 2, 4, 8. Column addresses are segmented by the burst length and serial data accesses are done within this boundary. The first column address to be accessed is supplied at the CAS timing and the subsequent addresses are generated automatically by the programmed burst length and its sequence. For example, in a burst length of 8 with interleave sequence, if the first address is ‘2’, then the rest of the burst sequence is 3, 0, 1, 6, 7, 4, and 5.

Address Input for Mode Set (Mode Register Operation)



Operation Mode

BA1	BA0	An~A10	A9	A8	A7	Mode
0	0	0	0	0	0	Burst Read/Burst Write
0	0	0	1	0	0	Burst Read/Single Write

Burst Type

A3	Type
0	Sequential
1	Interleave

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserve
0	0	1	Reserve
0	1	0	2
0	1	1	3
1	0	0	Reserve
1	0	1	Reserve
1	1	0	Reserve
1	1	1	Reserve

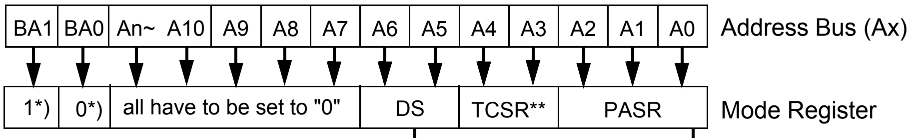
Burst Length

A2	A1	A0	Length	
			Sequential	Interleave
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full page	Reserve

Similar to the page mode of conventional DRAM's, burst read or write accesses on any column address are possible once the RAS cycle latches the sense amplifiers. The maximum t_{RAS} or the refresh interval time limits the number of random column accesses. A new burst access can be done even before the previous burst ends. The interrupt operation at every clock cycles is supported. When the previous burst is interrupted, the remaining addresses are overridden by the new address with the full burst length. An interrupt which accompanies with an operation change from a read to a write is possible by exploiting DQM to avoid bus contention.

When two or more banks are activated sequentially, interleaved bank read or write operations are possible. With the programmed burst length, alternate access and pre-charge operations on two or more banks can realize fast serial data access modes among many different pages. Once two or more banks are activated, column to column interleave operation can be done between different pages.

Extended Mode Register Table



Drive Strength

A6	A5	Drive Strength
0	0	Full
0	1	1/2
1	0	1/4
1	1	3/4

Partial-Array Self Refresh:

A2	A1	A0	banks to be self-refreshed
0	0	0	all banks
0	0	1	1/2 array (BA1=0)
0	1	0	1/4 array (BA1=0, BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array (BA1=BA0=0, RA11=0)
1	1	0	1/16 array (BA1=BA0=0, RA11=RA10=0)
1	1	1	Reserved

* *On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.
*)BA1 and BA0 must be 1, 0 to select the Extended Mode Register (Vs. the Mode Register)

The extended Mode Register can be set during the initialization sequence. Once the device is operational, the extended Mode Register set can be issued anytime when the part is idle.

Extended grade does not guarantee self-refresh function.

Burst Length and Sequence:

Burst Length	Starting Address (A2 A1 A0)	Sequential Burst Addressing (decimal)	Interleave Burst Addressing (decimal)
2	xx0 xx1	0, 1 1, 0	0, 1 1, 0
4	x00 x01 x10 x11	0, 1, 2, 3 1, 2, 3, 0 2, 3, 0, 1 3, 0, 1, 2	0, 1, 2, 3 1, 0, 3, 2 2, 3, 0, 1 3, 2, 1, 0
8	000 001 010 011 100 101 110 111	0 1 2 3 4 5 6 7 1 2 3 4 5 6 7 0 2 3 4 5 6 7 0 1 3 4 5 6 7 0 1 2 4 5 6 7 0 1 2 3 5 6 7 0 1 2 3 4 6 7 0 1 2 3 4 5 7 0 1 2 3 4 5 6	0 1 2 3 4 5 6 7 1 0 3 2 5 4 7 6 2 3 0 1 6 7 4 5 3 2 1 0 7 6 5 4 4 5 6 7 0 1 2 3 5 4 7 6 1 0 3 2 6 7 4 5 2 3 0 1 7 6 5 4 3 2 1 0
Full Page	nnn	Cn, Cn+1, Cn+2	Not supported

Refresh Mode

SDRAM has two refresh modes, Auto Refresh and Self Refresh. Auto Refresh is similar to the $\overline{CAS}$ -before-$\overline{RAS}$ refresh of conventional DRAMs. All of banks must be precharged before applying any refresh mode. An on-chip address counter increments the word and the bank addresses and no bank information is required for both refresh modes.

The chip enters the Auto Refresh mode, when $\overline{RAS}$ and $\overline{CAS}$ are held low and CKE and $\overline{WE}$ are held high at a clock timing. The mode restores word line after the refresh and no external precharge command is necessary. A minimum t_{RC} time is required between two automatic refreshes in a burst refresh mode. The same rule applies to any access command after the automatic refresh operation.

The chip has an on-chip timer and the Self Refresh mode is available. It enters the mode when $\overline{RAS}$, $\overline{CAS}$, and CKE are low and $\overline{WE}$ is high at a clock timing. All of external control signals including the clock are disabled. Returning CKE to high enables the clock and initiates the refresh exit operation. After the exit command, at least one t_{RC} delay is required prior to any access command. Extended grade does not guarantee self-refresh function.

DQM Function

DQM has two functions for data I/O read and write operations. During reads, when it turns to “high” at a clock timing, data outputs are disabled and become high impedance after delay (DQM Data Disable Latency t_{DQZ}). It also provides a data mask function for writes. When DQM is activated, the write operation at the next clock is prohibited (DQM Write Mask Latency t_{DQW} = zero clocks).

Power Down

In order to reduce standby power consumption, a power down mode is available. All banks must be precharged and the necessary Precharge delay (t_{RP}) must occur before the SDRAM can enter the Power Down mode. Once the Power Down mode is initiated by holding CKE low, all of the receiver circuits except CLK and CKE are gated off. The Power Down mode does not perform any refresh operations, therefore the device can’t remain in Power Down mode longer than the Refresh period (t_{REF}) of the device. Exit from this mode is performed by taking CKE “high”. One clock delay is required for mode entry and exit.

Auto Precharge

Two methods are available to precharge SDRAMs. In an automatic precharge mode, the CAS timing accepts one extra address, CA10, to determine whether the chip restores or not after the operation. If CA10 is high when a Read Command is issued, the **Read with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation one clock before the last data out for $\overline{CAS}$ latencies 2, and two clocks for $\overline{CAS}$ latencies 3. If CA10 is high when a Write Command is issued, the **Write with Auto-Precharge** function is initiated. The SDRAM automatically enters the precharge operation a time delay equal to t_{WR} (Write recovery time) after the last data in.

Precharge Command

There is also a separate precharge command available. When $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at a clock timing, it triggers the precharge operation. Three address bits, BA0, BA1 and A10 are used to define banks as shown in the following list. The precharge command can be imposed one clock before the last data out for CAS latency = 2, two clocks before the last data out for CAS latency = 3. Writes require a time delay twr from the last data out to apply the precharge command.

Bank Selection by Address Bits:

A10	BA0	BA1	
0	0	0	Bank 0
0	0	1	Bank 1
0	1	0	Bank 2
0	1	1	Bank 3
1	X	X	all Banks

Burst Termination

Once a burst read or write operation has been initiated, there are several methods in which to terminate the burst operation prematurely. These methods include using another Read or Write Command to interrupt an existing burst operation, use a Pre-charge Command to interrupt a burst cycle and close the active bank, or using the Burst Stop Command to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank. When interrupting a burst with another Read or Write Command care must be taken to avoid I/O contention. The Burst Stop Command, however, has the fewest restrictions making it the easiest method to use when terminating a burst operation before it has been completed. If a Burst Stop command is issued during a burst write operation, then any residual data from the burst write cycle will be ignored. Data that is presented on the I/O pins before the Burst Stop Command is registered will be written to the memory.

Deep Power Down Mode

The Deep Power Down mode is an unique
with very low standby currents. All internal voltage generators inside the Mobile SDRAM are stopped; all memory data is lost in this mode. To enter the Deep Power Down mode all banks must be precharged

Recommended Operation and Characteristics

T_A = -25 to 85 °C(Commercial); -40 to 125°C(Extended) V_{SS} = 0 V; V_{DD}= 1.8 V,V_{DDQ} = 1.8V

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Supply voltage	V_{DD}	1.7	1.95	V	
I/O Supply Voltage	V_{DDQ}	1.7	1.95	V	1, 2
Input high voltage (AC)	V_{IH}	0.8xV_{DDQ}	V_{DD}+0.3	V	1, 2
Input low voltage (AC)	V_{IL}	– 0.3	0.3	V	1, 2
Output high voltage (I_{OUT} = – 0.1 mA)	V_{OH}	0.9*V_{CCQ}	–	V	
Output low voltage (I_{OUT} = 0.1 mA)	V_{OL}	–	0.2	V	
Input leakage current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	– 1	1	µA	
Output leakage current (DQ is disabled, 0 V < V_{OUT} < V_{CC})	$I_{O(L)}$	– 1.5	1.5	µA	

Note:
1. All voltages are referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2 V for pulse width of < 3ns with 1.8V. V_{IL} may undershoot to -2 V for pulse width < 3ns with 1.8V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

*Absolute Maximum Ratings**

Operating temperature range (commercial)-25 to 85 °C
Operating temperature range (industrial) -40 to 85 °C
Storage temperature range .... -55 to 150 °C
Input/output voltage .... -0.5 to 2.4 V
Power supply voltage .... -0.5 to 2.4 V

***Note:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage of the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Currents T_A =-25 to 85 °C(Commercial)/-40 to 85 °C(Industrial);

V_{SS} = 0 V; V_{DD}= 1.8 V,V_{DDQ} = 1.8V(Recommended Operating Conditions unless otherwise noted)

Symbol	Parameter & Test Condition		Max. -6	Max. -7	Unit	Note
ICC1	Operating Current $t_{RC} = t_{RCMIN.}$, $t_{RC} = t_{CKMIN.}$ Active-precharge command cycling, without Burst Operation	1 bank operation	50	45	mA	7
ICC2P	Precharge Standby Current in Power Down Mode $\overline{CS}$ =V_{IH}, CKE≤ $V_{IL(max)}$	t_{CK} = min.	0.3	0.3	mA	7
ICC2N	Precharge Standby Current in Non-Power Down Mode $\overline{CS}$ =V_{IH}, CKE≥ $V_{IL(max)}$	t_{CK} = min.	10	10	mA	
ICC3N	No Operating Current t_{CK} = min, $\overline{CS}$ = $V_{IH(min)}$ bank ; active state (4 banks)	CKE ≥ $V_{IH(MIN.)}$	20	20	mA	
ICC3P		CKE ≤ $V_{IL(MAX.)}$ (Power down mode)	5	5	mA	
ICC4	Burst Operating Current t_{CK} = min Read/Write command cycling		75	70	mA	7,8
ICC5	Auto Refresh Current t_{CK} = min Auto Refresh command cycling		95	95	mA	7
IZZ	Deep Power Down Current		10	10	uA	

Notes:

7. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}.
8. These parameter depend on output loading. Specified values are obtained with output open.

Temperature Compensated/Partial Array Self-Refresh Currents

Parameter & Test Condition	Extended Mode Register A[2:0] Tcase [^oC]	Symb.	max.	Unit	Note
Self Refresh Current Self Refresh Mode CKE=Low, tck=min, full array activations, all banks	85^oC max.	ICC6	600	uA	
	45^oC max.	ICC6	300	uA	
Self Refresh Current Self Refresh Mode CKE=Low, tck=min, 1/2 array activations	85^oC max.	ICC6	480	uA	
	45^oC max.	ICC6	260	uA	
Self Refresh Current Self Refresh Mode CKE=Low, tck=min, 1/4 array activation	85^oC max.	ICC6	420	uA	
	45^oC max.	ICC6	250	uA	
Self Refresh Current Self Refresh Mode CKE=Low, tck=min, 1/8 array activation	85^oC max.	ICC6	420	uA	
	45^oC max.	ICC6	250	uA	
Self Refresh Current Self Refresh Mode CKE=Low, tck=min, 1/16 array activation	85^oC max.	ICC6	400	uA	
	45^oC max.	ICC6	250	uA	

AC Characteristics

T_A = -25 to 85 °C(Commercial)/-40 to 85 °C(Industrial) V_{SS} = 0 V; V_{DD}= 1.8 V,V_{DDQ} = 1.8V, t_T=1 ns

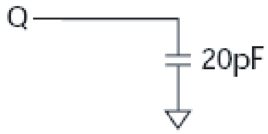
#	Symbol	Parameter	Limit Values -6 Min.	-6 Max.	-7 Min.	-7 Max.	Unit	Note
Clock and Clock Enable								
1	t_{CK}	Clock Cycle Time $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 6 9	 – –	 7.5 9	 – –	 ns ns	 6
2	f_{CK}	Clock Frequency $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 – –	 166 110	 – –	 133 110	 MHz MHz	
3	t_{AC}	Access Time from Clock $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	 – –	 5 8	 – –	 5.4 8	 ns ns	
4	t_{CH}	Clock High Pulse Width	2.5	–	2.5	–	ns	
5	t_{CL}	Clock Low Pulse Width	2.5	–	2.5	–	ns	
6	t_T	Transition Tim	0.3	1.2	0.3	1.2	ns	9
Setup and Hold Times								
7	t_{CKH}	CKE hold time	1	–	1	–	ns	
8	t_{CKS}	CKE setup time	1.5	–	1.5	–	ns	
9	t_{DH}	Data-in hold time	1	–	1	–	ns	
10	t_{DS}	Data-in setup time	1.5	–	1.5	–	ns	
11	t_{AH}	Address hold time	1	–	1	–	ns	
12	t_{AS}	Address setup time	1.5	–	1.5	–	ns	
13	t_{CMH}	/CS, /RAS, /CAS, /WE, DQM hold time	1.5		1.5	–	ns	
14	t_{CMS}	/CS, /RAS, /CAS, /WE, DQM setup time	0.5	–	0.5	–	ns	
15	t_{MRD}	Mode Register Set to Command delay	2	–	2	–	CLK	
Common Parameters								
16	t_{RCD}	Row to Column Delay Time	18	–	19.2	–	ns	
17	t_{RP}	Row Precharge Time	18	–	19.2	–	ns	
18	t_{RAS}	Row Active Time	42	100K	45	100k	ns	
19	t_{RC}	Active to Active/Auto Refresh command period	60	–	67.5	–	ns	
20	t_{RRD}	Activate(a) to Activate(b) Command Period	2	–	2	–	CLK	
21	t_{BDL}	Last data-in to burst STOP command	1	–	1	–	CLK	12
22	t_{CCD}	$\overline{CAS}$(a) to $\overline{CAS}$(b) Command Period	1	–	1	–	CLK	12
23	t_{CDL}	Last data-in to new READ/WRITE command	1	–	1	–	CLK	13

AC Characteristics (Cont'd)

#	Symbol	Parameter	Limit Values				Unit	Note
			-6		-7			
			Min.	Max.	Min.	Max.		
24	t_{CKED}	CKE to clock disable or power-down entry mode	1	–	1	–	CLK	13
25	t_{PED}	CKE to clock enable or power-down exit mode	1	–	1	–	CLK	13
Refresh Cycle								
26	t_{REF}	Refresh Period (8192 cycles)	—	64	—	64	ms	8
27	t_{XSR}	Exit SELF REFRESH to first valid command	112	—	112.5	—	ns	11
28	t_{RFC}	Row Refresh Cycle Time	97.5	–	97.5	–	ns	
Read Cycle								
29	t_{OH}	Data Out Hold Time(load)	2.5	–	2.5	–	ns	
30	t_{OHN}	Data Out Hold Time(no load)	1.8	–	1.8	–	ns	
31	t_{LZ}	Data Out to Low Impedance Time	1	–	1	–	ns	7
32	t_{HZ}	Data Out to High Impedance Time $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	– –	5 8	– –	5.4 8	ns ns	
33	t_{ROH}	Data-out High-Z from PRECHARGE command $\overline{CAS}$ Latency = 3 $\overline{CAS}$ Latency = 2	3 2	– –	3 2	– –	CLK CLK	12
Write Cycle								
34	t_{WR}	Write Recovery Time	15	–	15	–	ns	10
35	t_{DAL}	Data-in to ACTIVE command	5	–	5	–	CLK	14,16
36	t_{DPL}	Data-in to PRECHARGE command	2	–	2	–	CLK	15,16
37	t_{DQD}	DQM to input data delay	0	–	0	–	CLK	12
38	t_{DQM}	DQM to data mask during WRITEs	0	–	0	–	CLK	12
39	t_{DQZ}	DQM to data High-Z during READs	2	–	2	–	CLK	12
40	t_{DWD}	WRITE command to input data delay	0	–	0	–	CLK	12
41	t_{RDL}	Last data-in to PRECHARGE command	2	–	2	–	CLK	15,16

Note:

1. A full initialization sequence is required before proper device operation is ensured.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0^{o}C <$ TA $< +70^{o}C$ standard temperature and $-40^{o}C <$ TA $< +85^{o}C$ industrial temperature) is ensured.
3. In addition to meeting the transition rate specification, the clock and CKE must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
4. Outputs measured for 1.8V at 0.9V with equivalent load:



Test loads with full DQ driver strength. Performance will vary with actual system DQ bus capacitive loading, termination, and programmed drive strength.
5. AC timing tests have VIL and Vih with timing referenced to VIH/2 = crossover point. If the input transition time is longer than tT (MAX), then the timing is referenced at VIL (MAX) and VIH (MIN) and no longer at the VIH/2 crossover point.
6. The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock ball) during access or pre-charge states (READ, WRITE, including tWR, and PRE-CHARGE commands). CKE may be used to reduce the data rate.
7. tHZ defines the time at which the output achieves the open circuit condition, it is not a reference to VOH or VOL. The last valid data element will meet tOH before going High-Z.
8. The 512M Mobile SDRAM requires 8,192 AUTO REFRESH cycles every 64ms (tREF). Providing a distributed AUTO REFRESH command every 7.8125gs meets the refresh requirement and ensures that each row is refreshed. Alternatively, 8,192 AUTO REFRESH commands can be issued in a burst at the minimum cycle rate (tRFC), once every 64ms.
9. AC characteristics assume tT = 1ns.
10. Auto pre-charge mode only. The pre-charge timing budget (tRP) begins at x ns for -7 after the first clock delay and after the last WRITE is executed. May not exceed the limit set for pre-charge mode.
11. CLK must be toggled a minimum of two times during this period.
12. Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
13. Timing is specified by tCKS. Clock(s) specified as a reference only at minimum cycle rate.
14. Timing is specified by tWR plus tRP. Clock(s) specified as a reference only at minimum cycle rate.
15. Timing is specified by tWR. 16. Based on tCK (MIN), CL = 3.

Timing Diagrams

1. Bank Activate Command Cycle
2. Burst Read Operation
3. Read Interrupted by a Read
4. Read to Write Interval
    - 4.1 Read to Write Interval
    - 4.2 Minimum Read to Write Interval
    - 4.3 Non-Minimum Read to Write Interval
5. Burst Write Operation
6. Write and Read Interrupt
    - 6.1 Write Interrupted by a Write
    - 6.2 Write Interrupted by Read
7. Burst Write & Read with Auto-Precharge
    - 7.1 Burst Write with Auto-Precharge
    - 7.2 Burst Read with Auto-Precharge
8. Burst Termination
    - 8.1 Termination of a Burst Write Operation
    - 8.2 Termination of a Burst Write Operation
9. AC- Parameters
    - 9.1 AC Parameters for a Write Timing
    - 9.2 AC Parameters for a Read Timing
10. Mode Register Set
11. Power on Sequence and Auto Refresh (CBR)
12. Power Down Mode
13. Self Refresh (Entry and Exit)
14. Auto Refresh (CBR)

Timing Diagrams (Cont'd)

15. Random Column Read (Page within same Bank)

    15.1 $\overline{\text{CAS}}$ Latency = 2

    15.2 $\overline{\text{CAS}}$ Latency = 3

16. Random Column Write (Page within same Bank)

    16.1 $\overline{\text{CAS}}$ Latency = 2

    16.2 $\overline{\text{CAS}}$ Latency = 3

17. Random Row Read (Interleaving Banks) with Precharge

    17.1 $\overline{\text{CAS}}$ Latency = 2

    17.2 $\overline{\text{CAS}}$ Latency = 3

18. Random Row Write (Interleaving Banks) with Precharge

    18.1 $\overline{\text{CAS}}$ Latency = 2

    18.2 $\overline{\text{CAS}}$ Latency = 3

19. Precharge Termination of a Burst

    19.1 $\overline{\text{CAS}}$ Latency = 2

    19.2 $\overline{\text{CAS}}$ Latency = 3

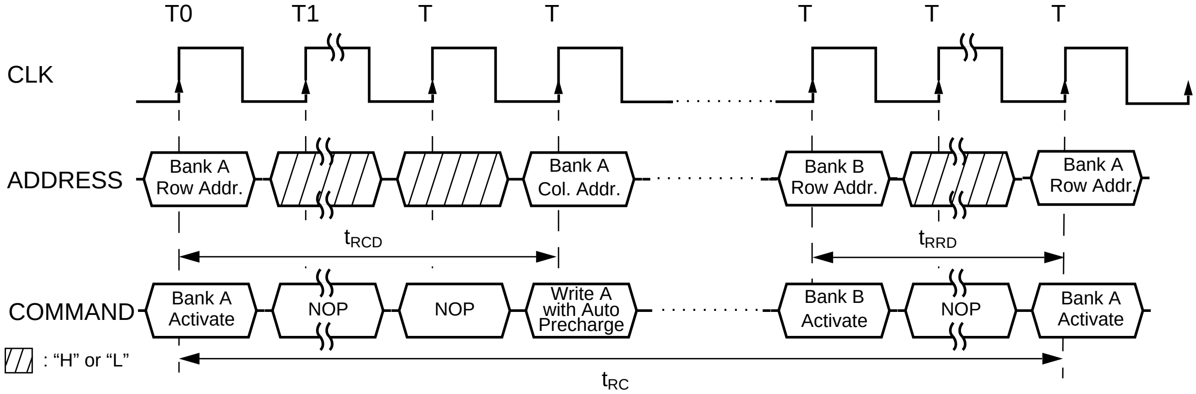
20. Deep Power Down Entry/Exit

    20.1 Deep Power Down Entry

    20.2 Deep Power Down Exit

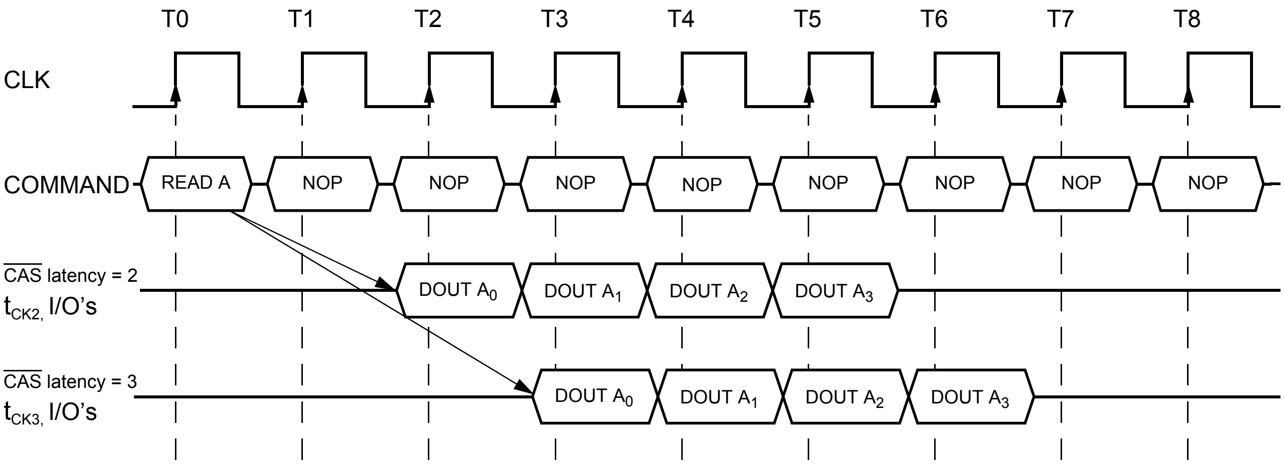
1. Bank Activate Command Cycle

($\overline{CAS}$ latency = 3)



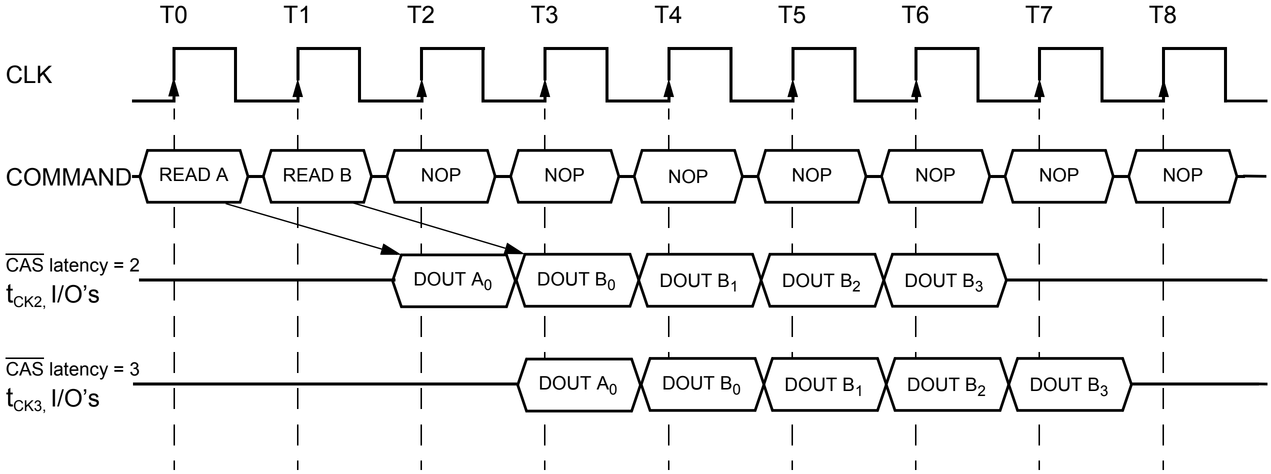
2. Burst Read Operation

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



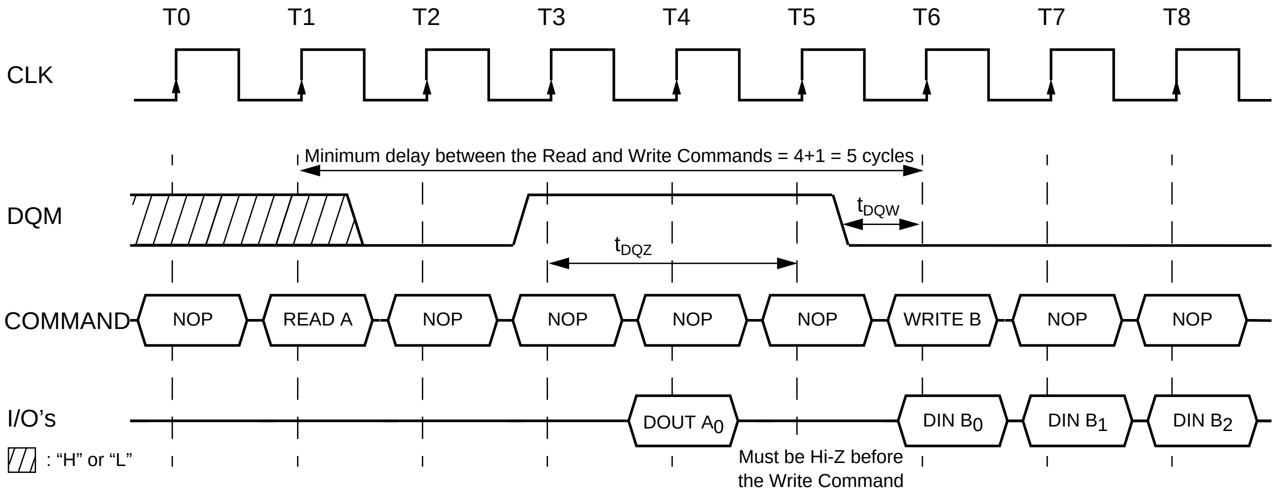
3. Read Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



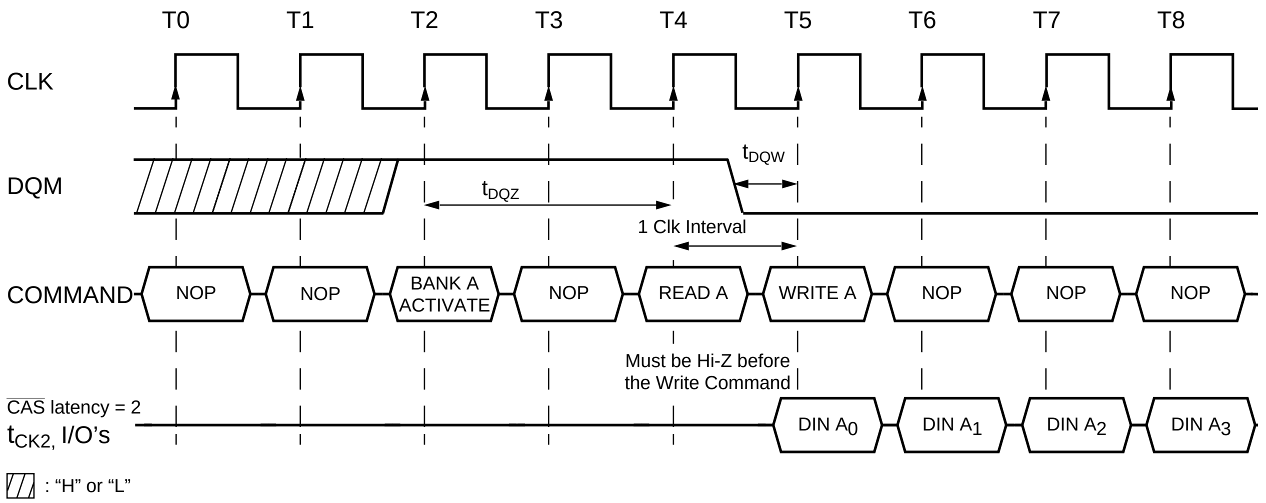
4.1 Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 3)



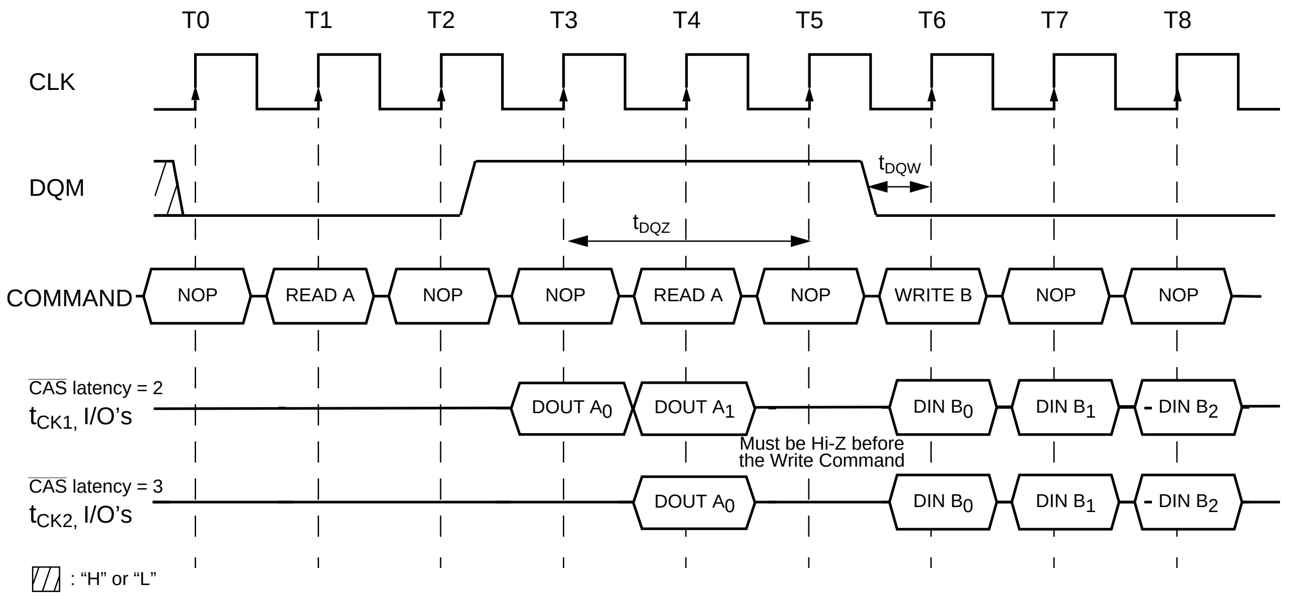
4.2 Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2)



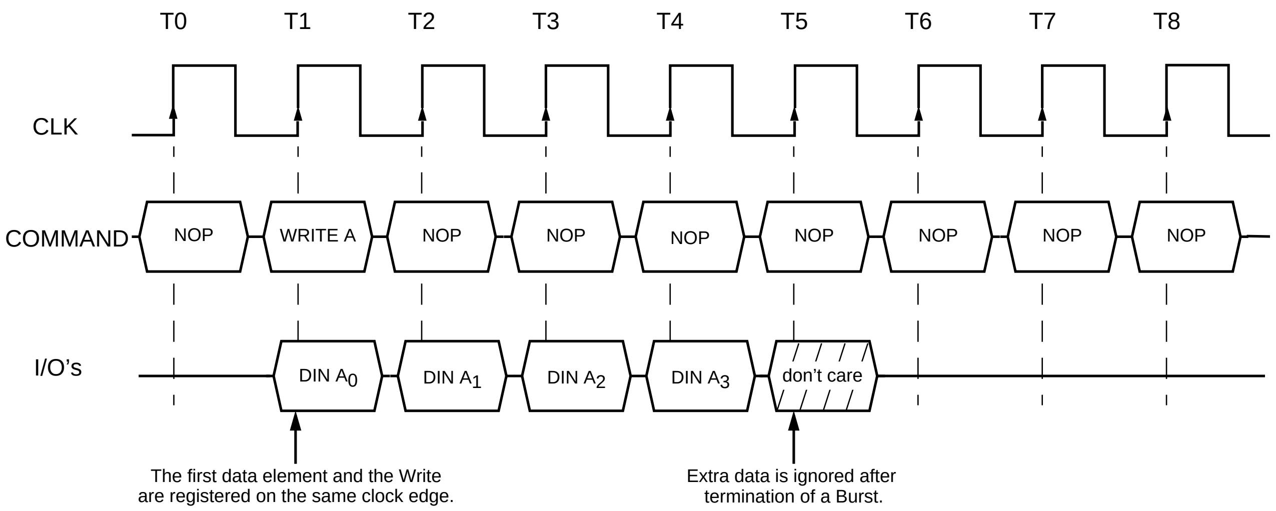
4.3 Non-Minimum Read to Write Interval

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



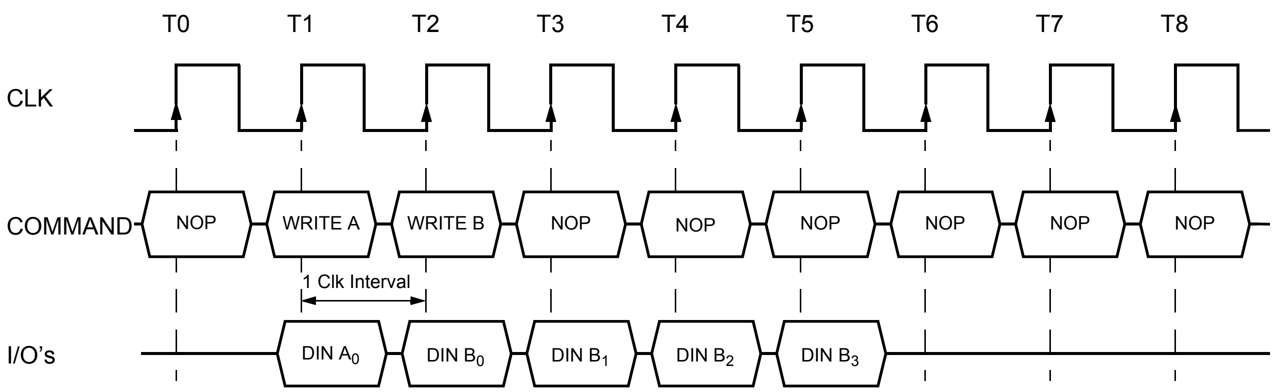
5. Burst Write Operation

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



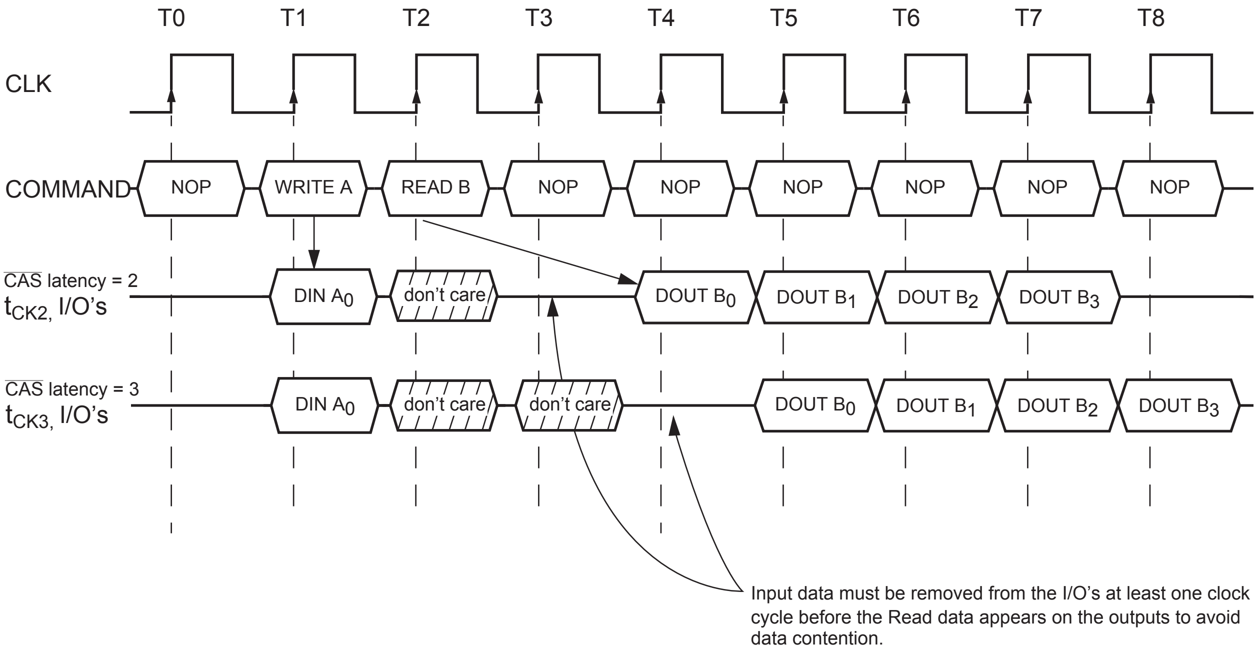
6.1 Write Interrupted by a Write

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



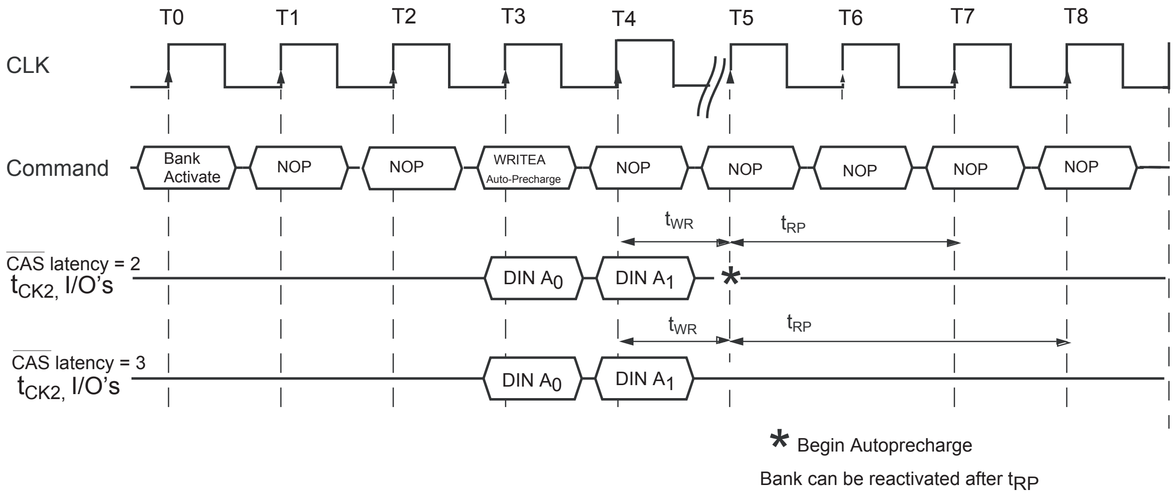
6.2 Write Interrupted by a Read

(Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



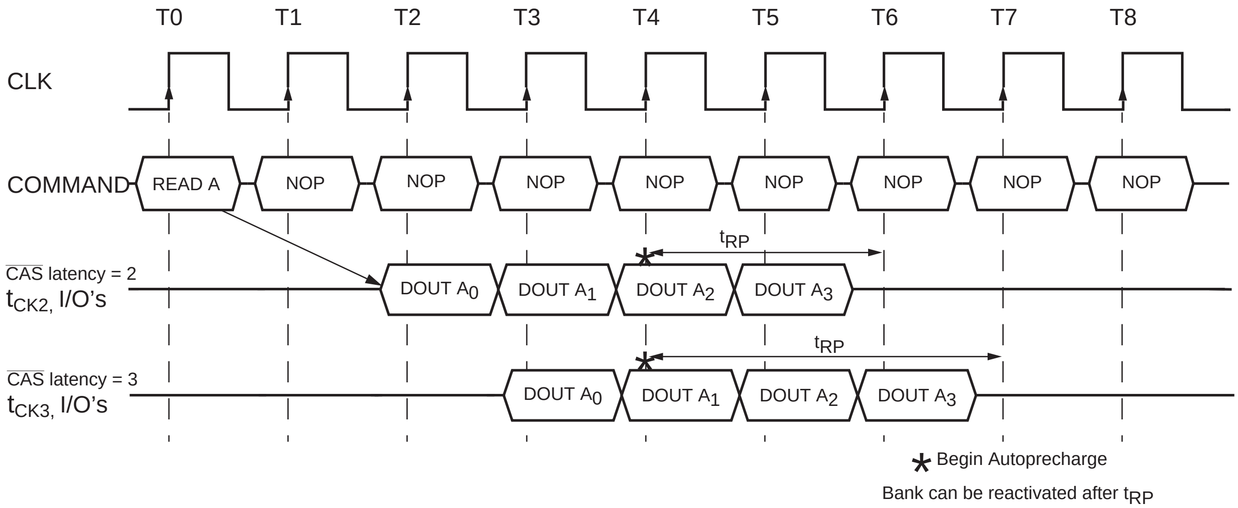
7. Burst Write with Auto-Precharge

Burst Length = 2, $\overline{CAS}$ latency = 2, 3)



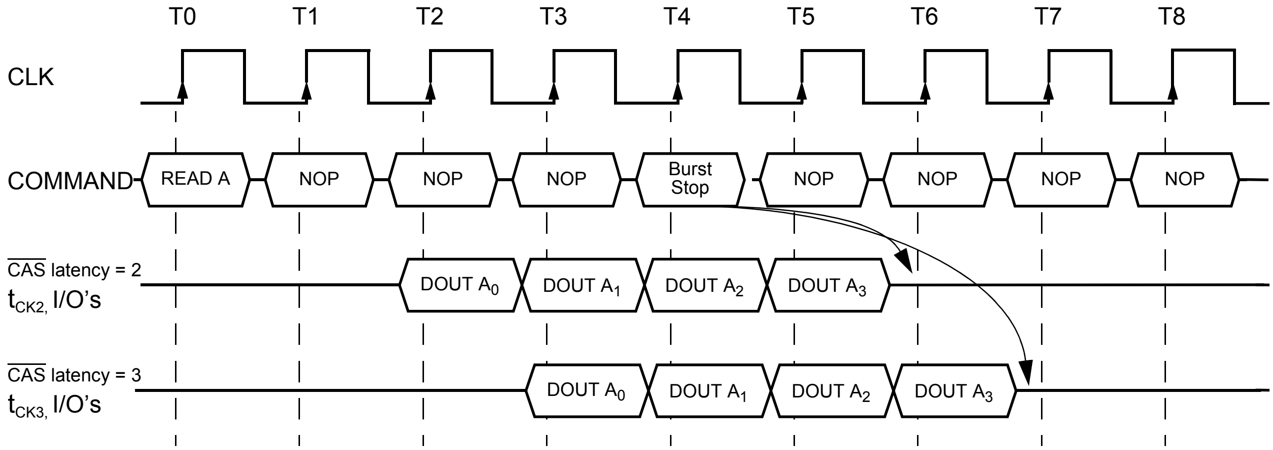
7.2 Burst Read with Auto-Precharge

Burst Length = 4, $\overline{CAS}$ latency = 2, 3)



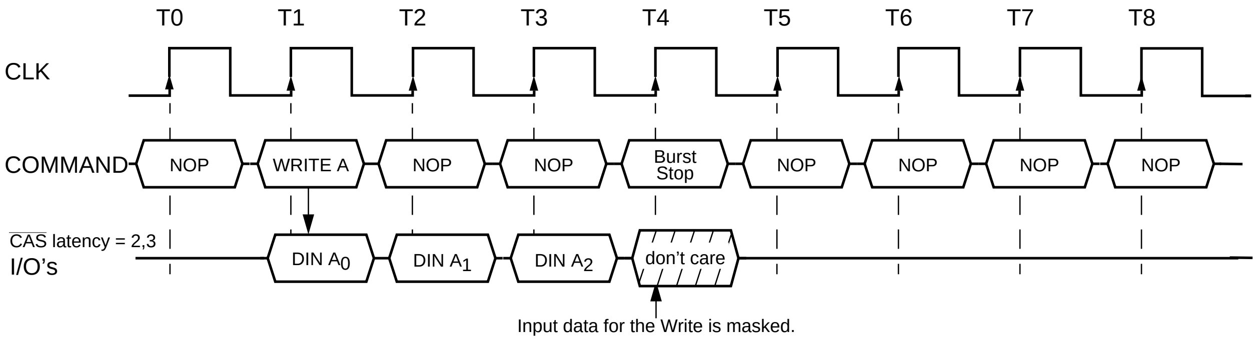
8.1 Termination of a Burst Read Operation

($\overline{CAS}$ latency = 2, 3)



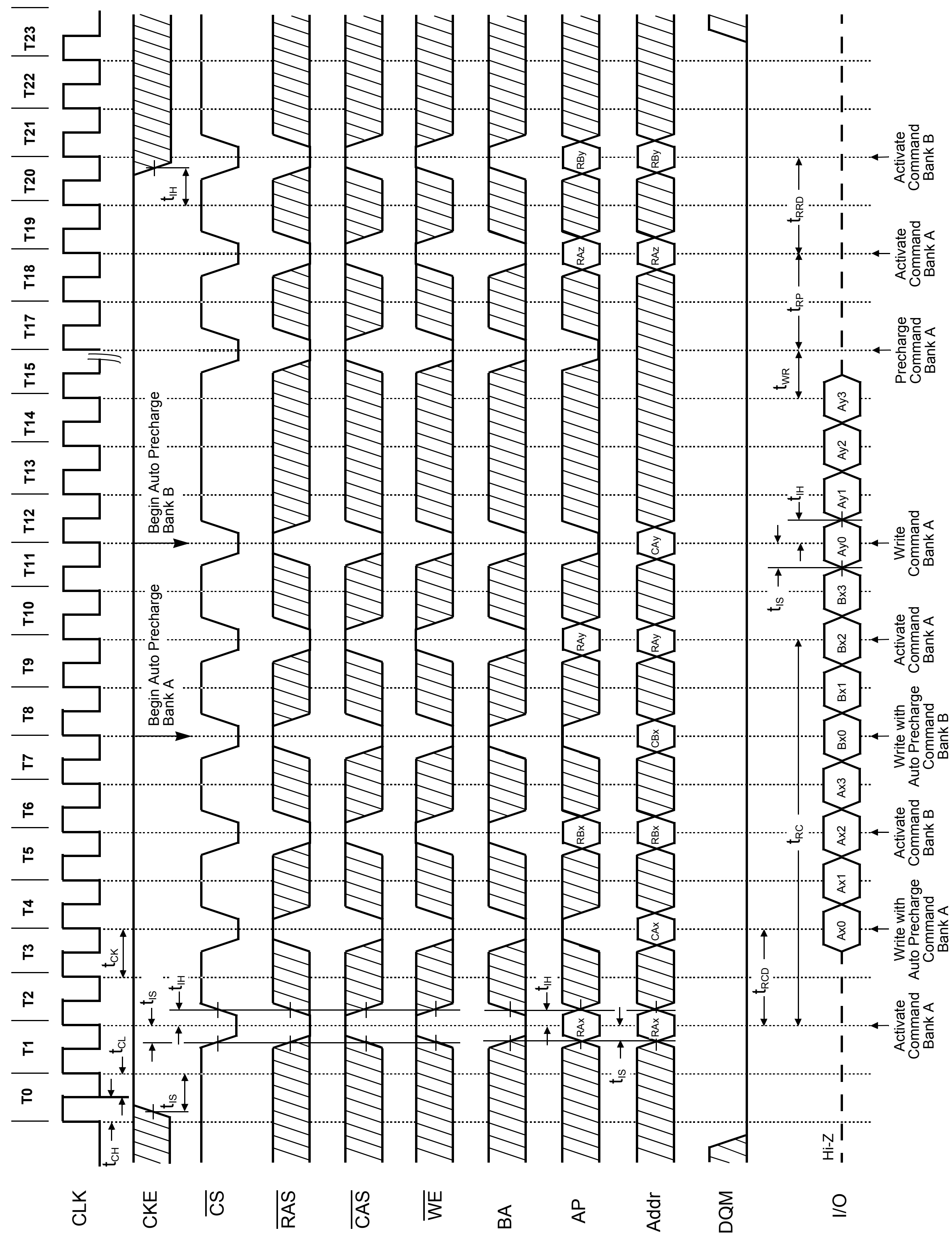
8.2 Termination of a Burst Write Operation

($\overline{CAS}$ latency = 2, 3)



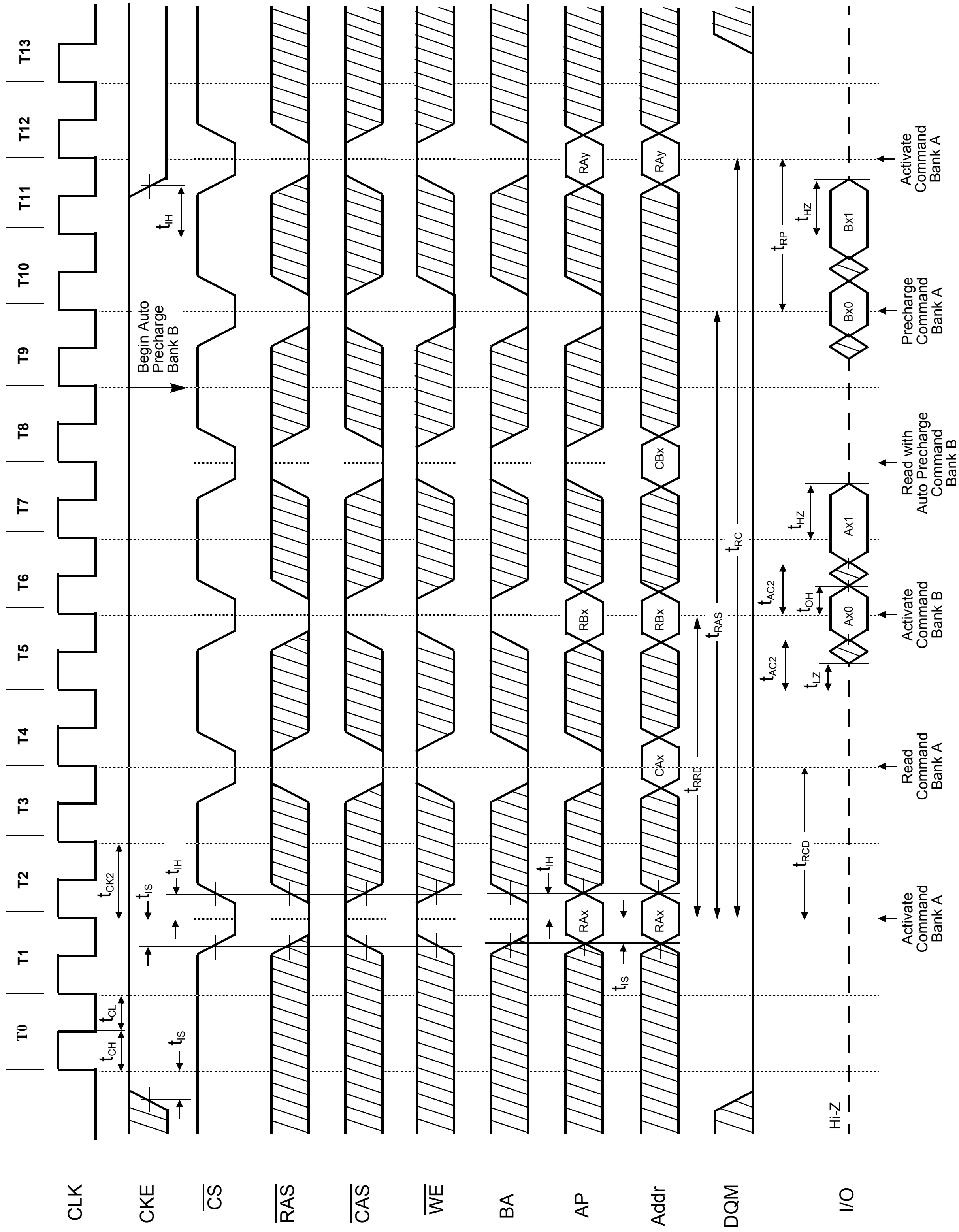
9.1 AC Parameters for Write Timing

Burst Length = 4, $\overline{CAS}$ Latency = 2

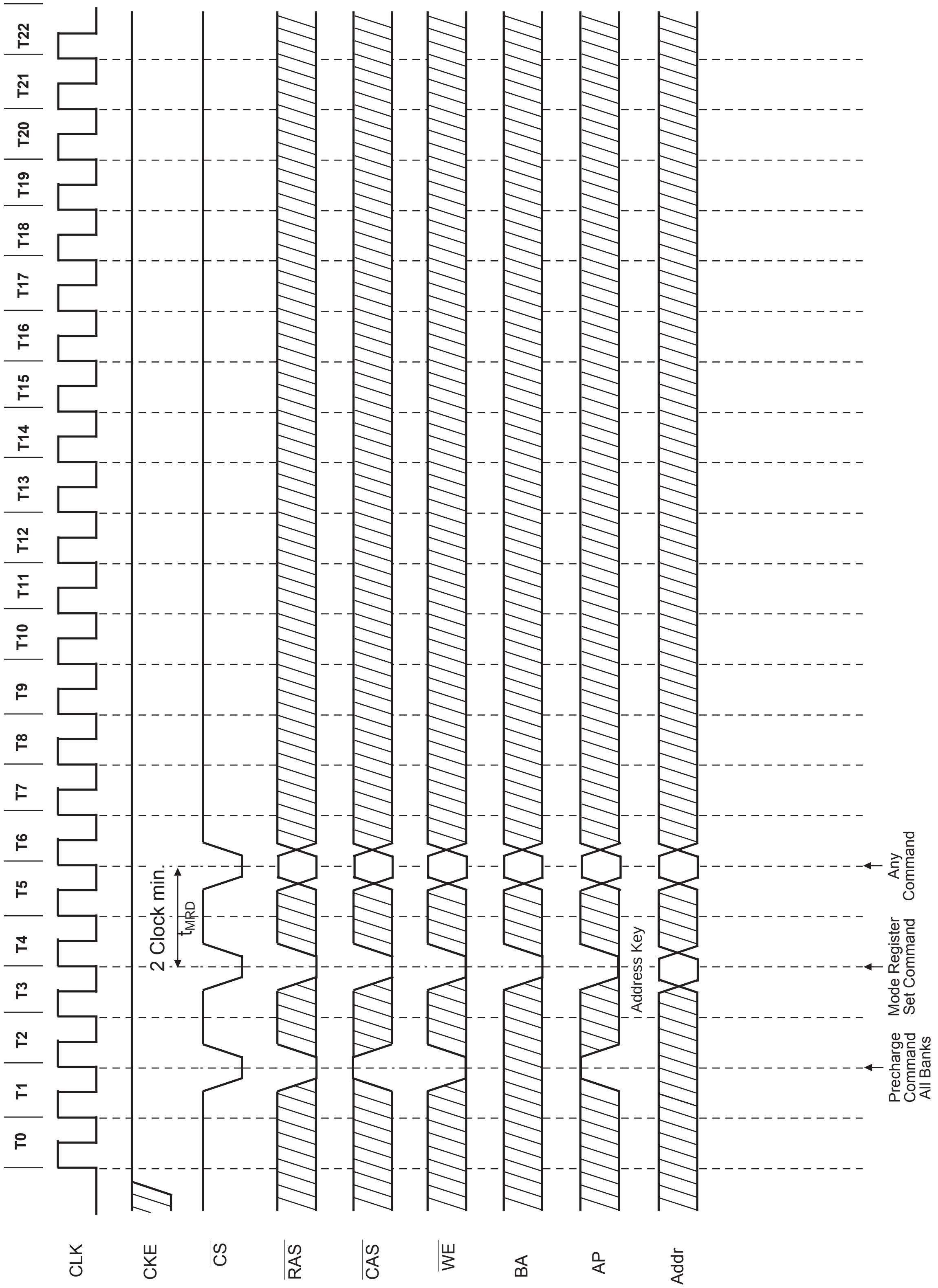


9.1 AC Parameters for Read Timing

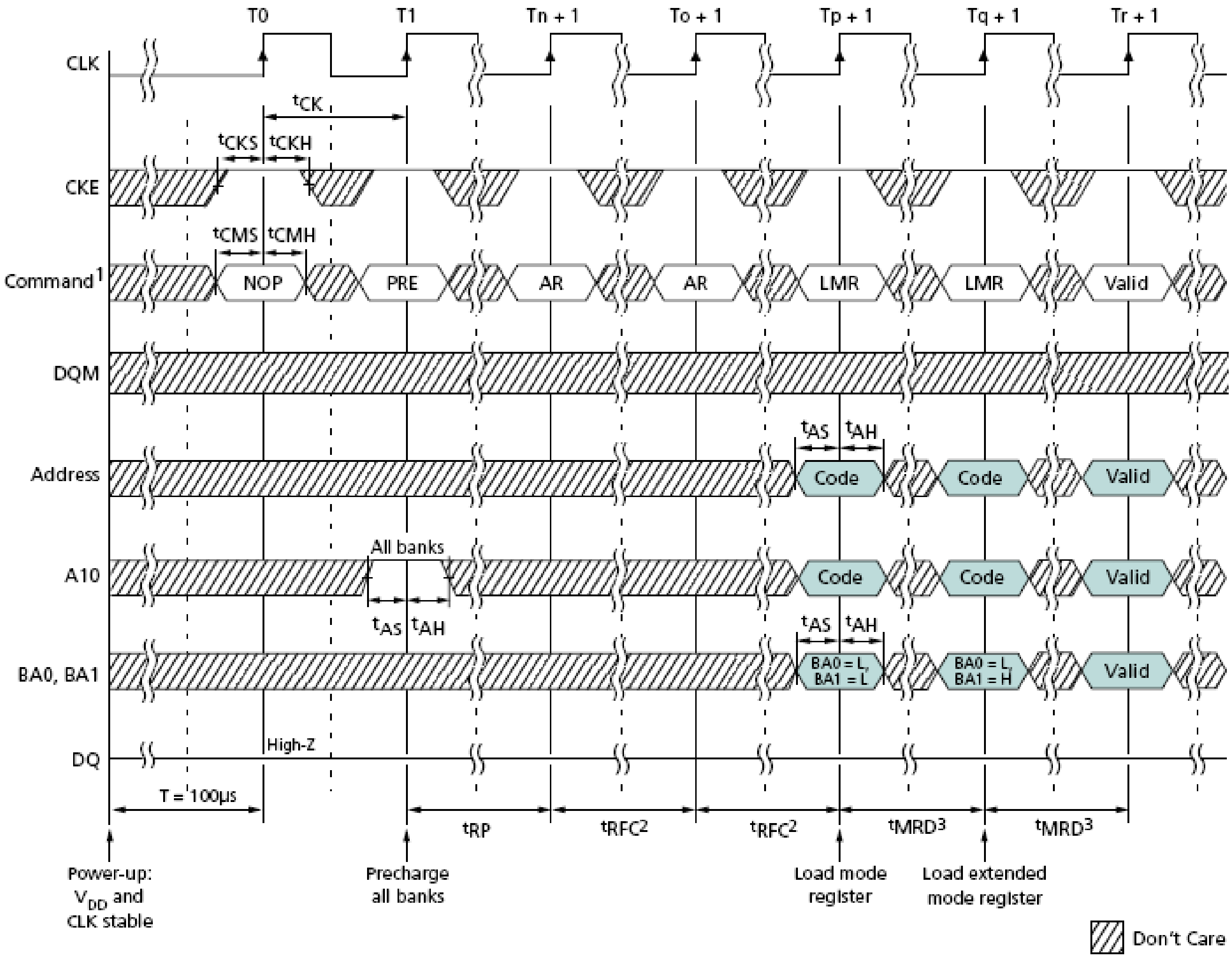
Burst Length = 2, $\overline{CAS}$ Latency = 2



10. Mode Register Set



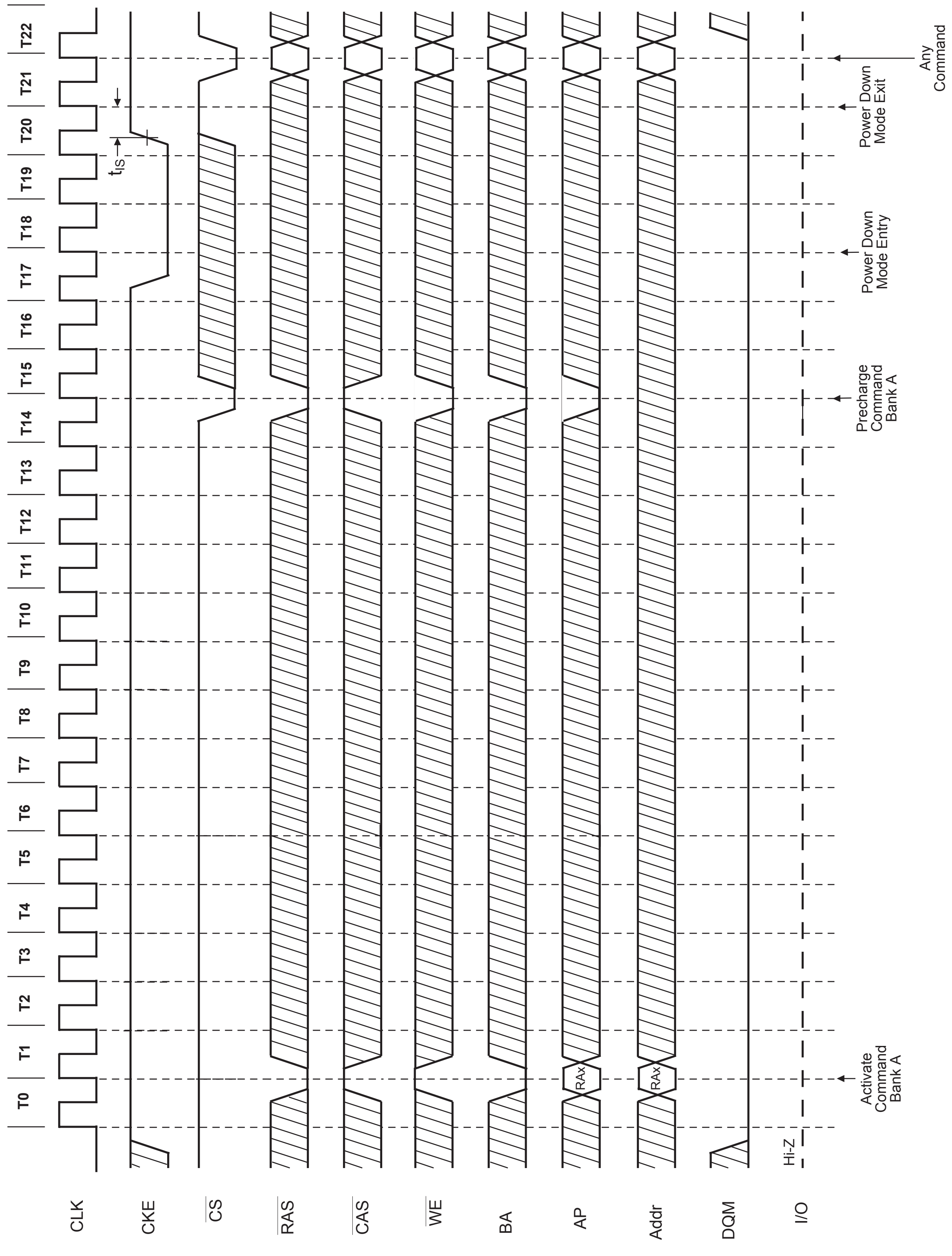
11. Power on Sequence and Auto Refresh (CBR)



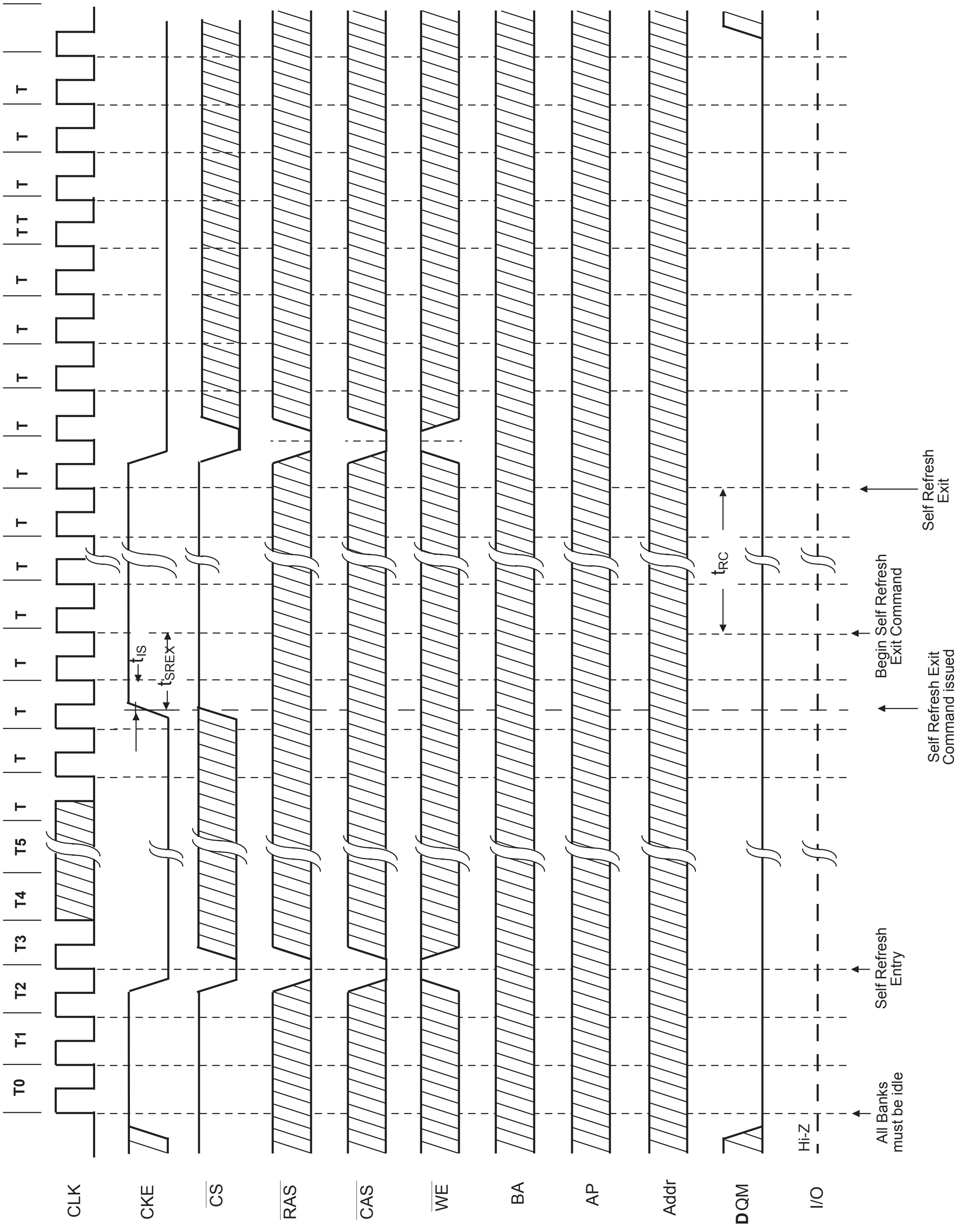
Notes:
1. PRE = PRECHARGE command, AR = AUTO REFRESH command, LMR = LOAD MODE REGISTER command.
2. NOPs or DESELECTs must only be provided during tRFC time.
3. NOPs or DESELECTs must only be provided during tMRD time.

12. Power Down Mode

Burst Length = 4, $\overline{CAS}$ Latency = 2

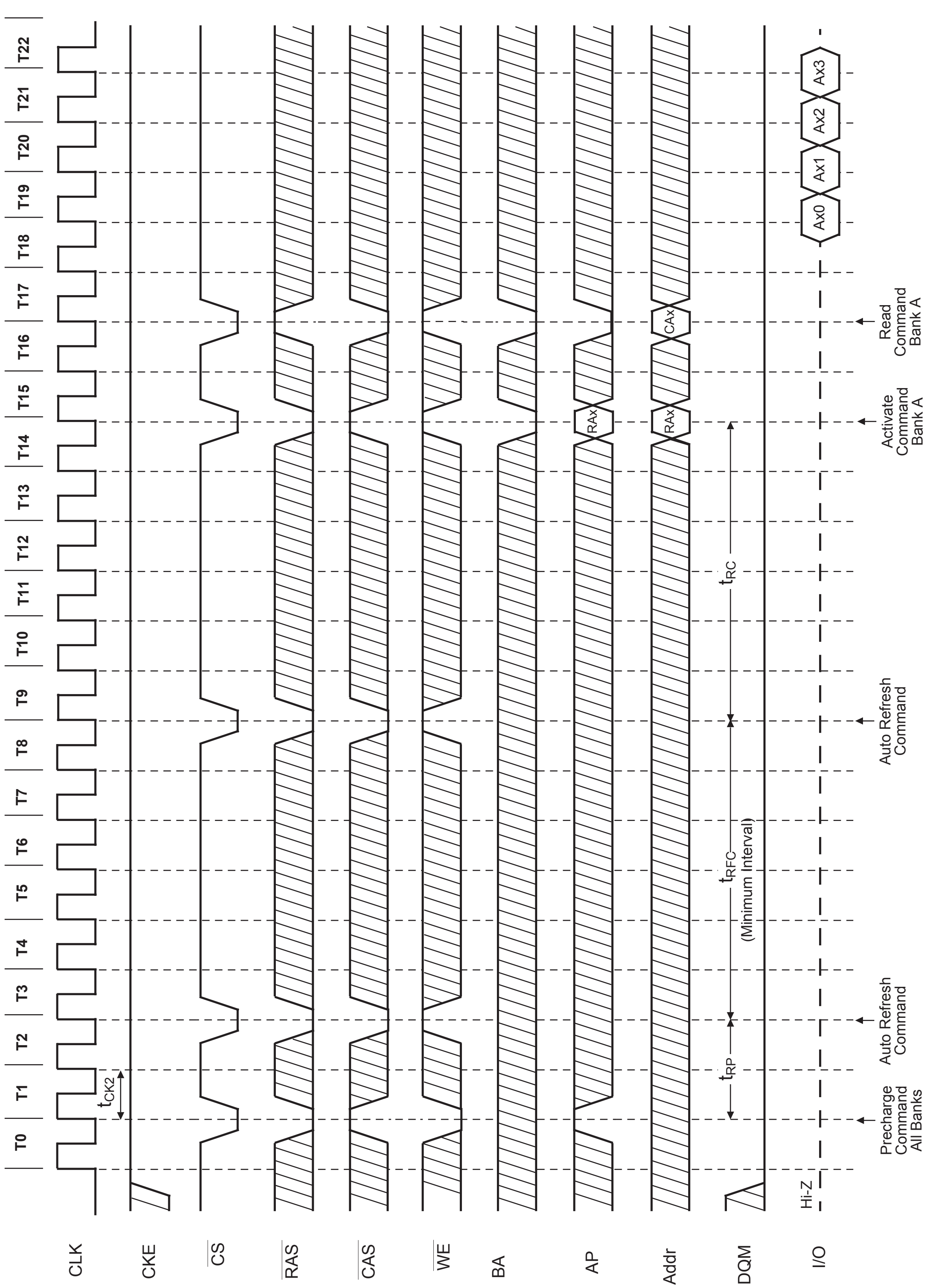


13. Self Refresh (Entry and Exit)



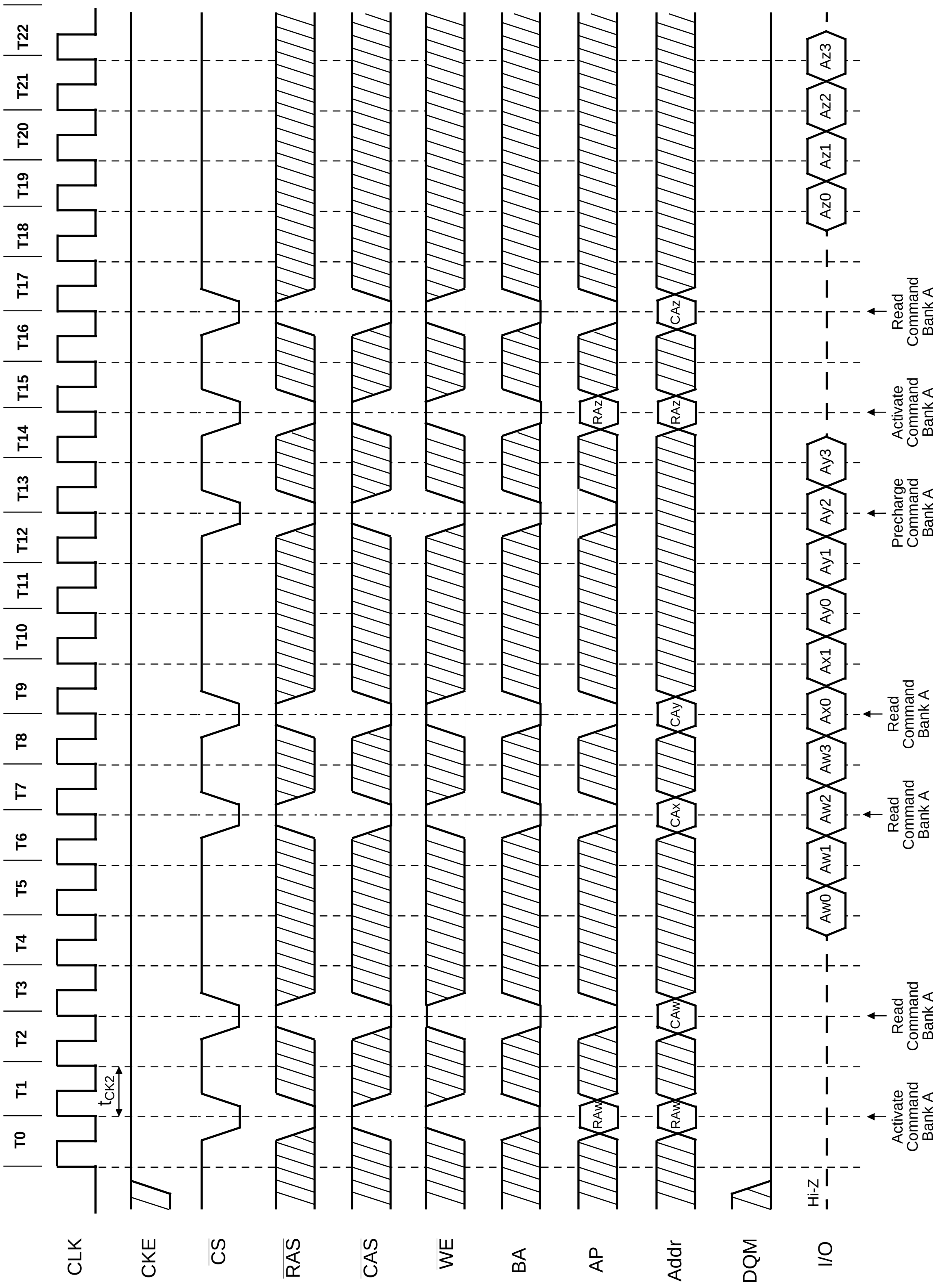
14. Auto Refresh (CBR)

Burst Length = 4, $\overline{CAS}$ Latency = 2

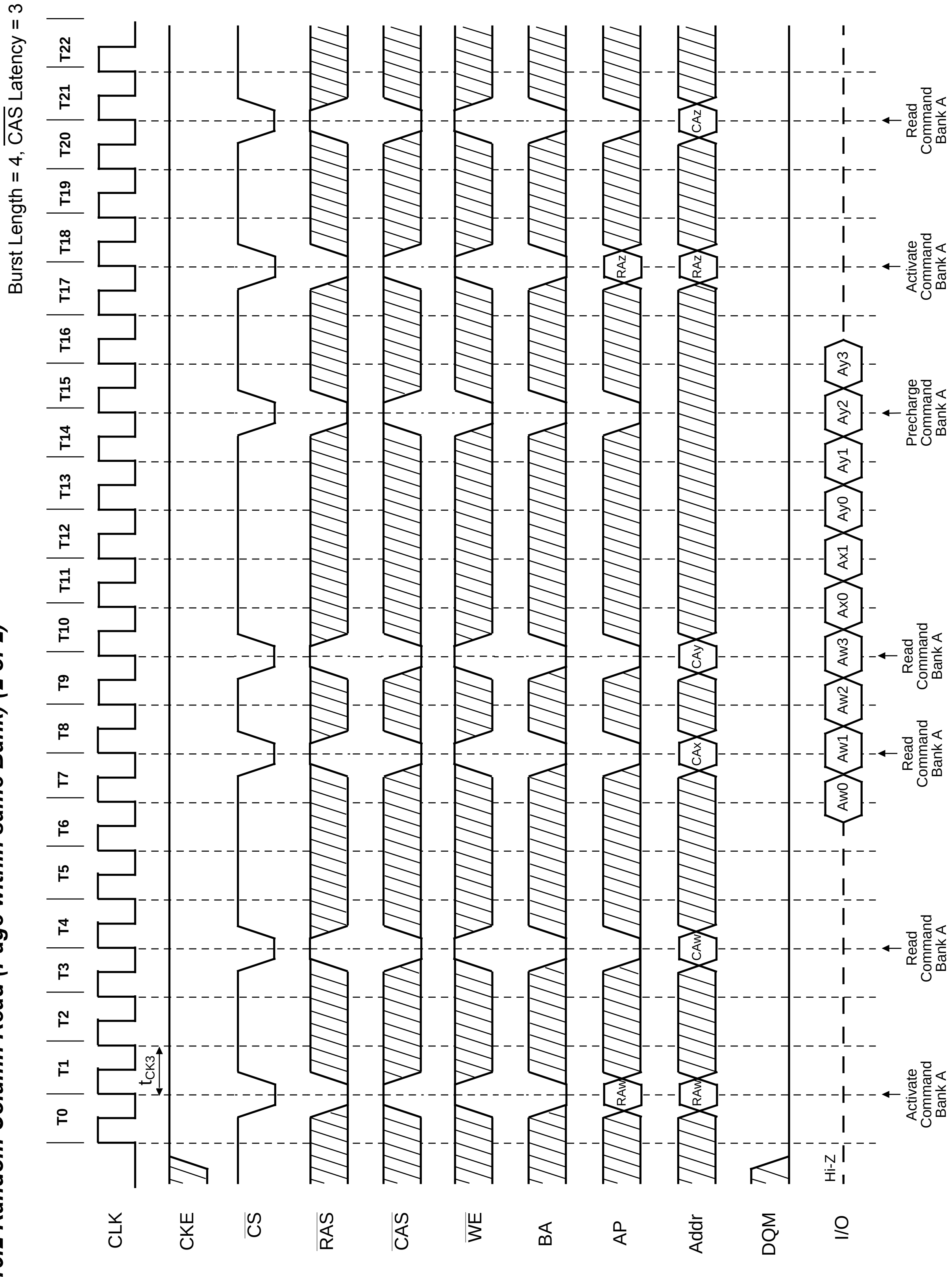


15.1 Random Column Read (Page within same Bank) (1 of 2)

Burst Length = 4, $\overline{CAS}$ Latency = 2

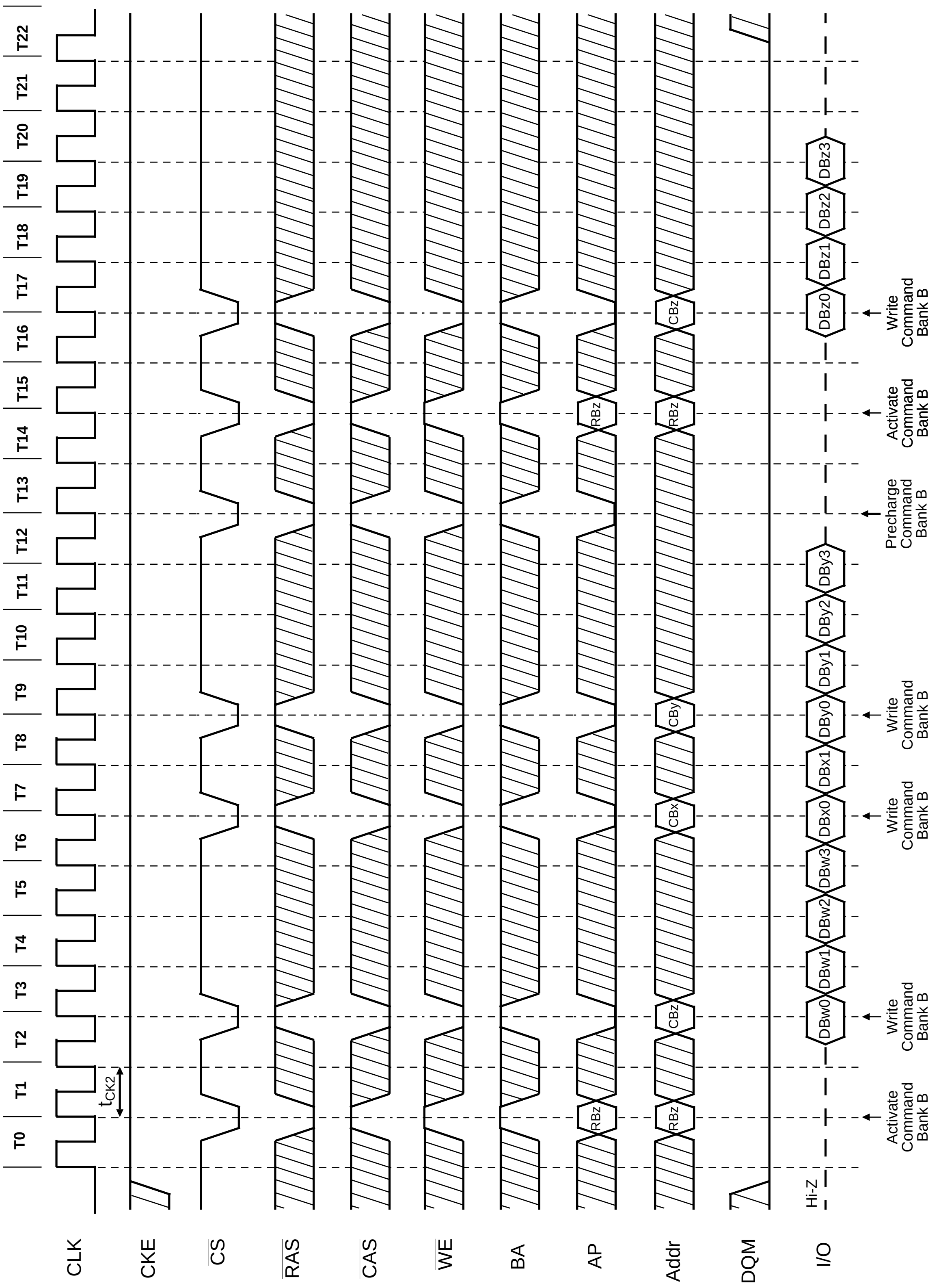


15.2 Random Column Read (Page within same Bank) (2 of 2)

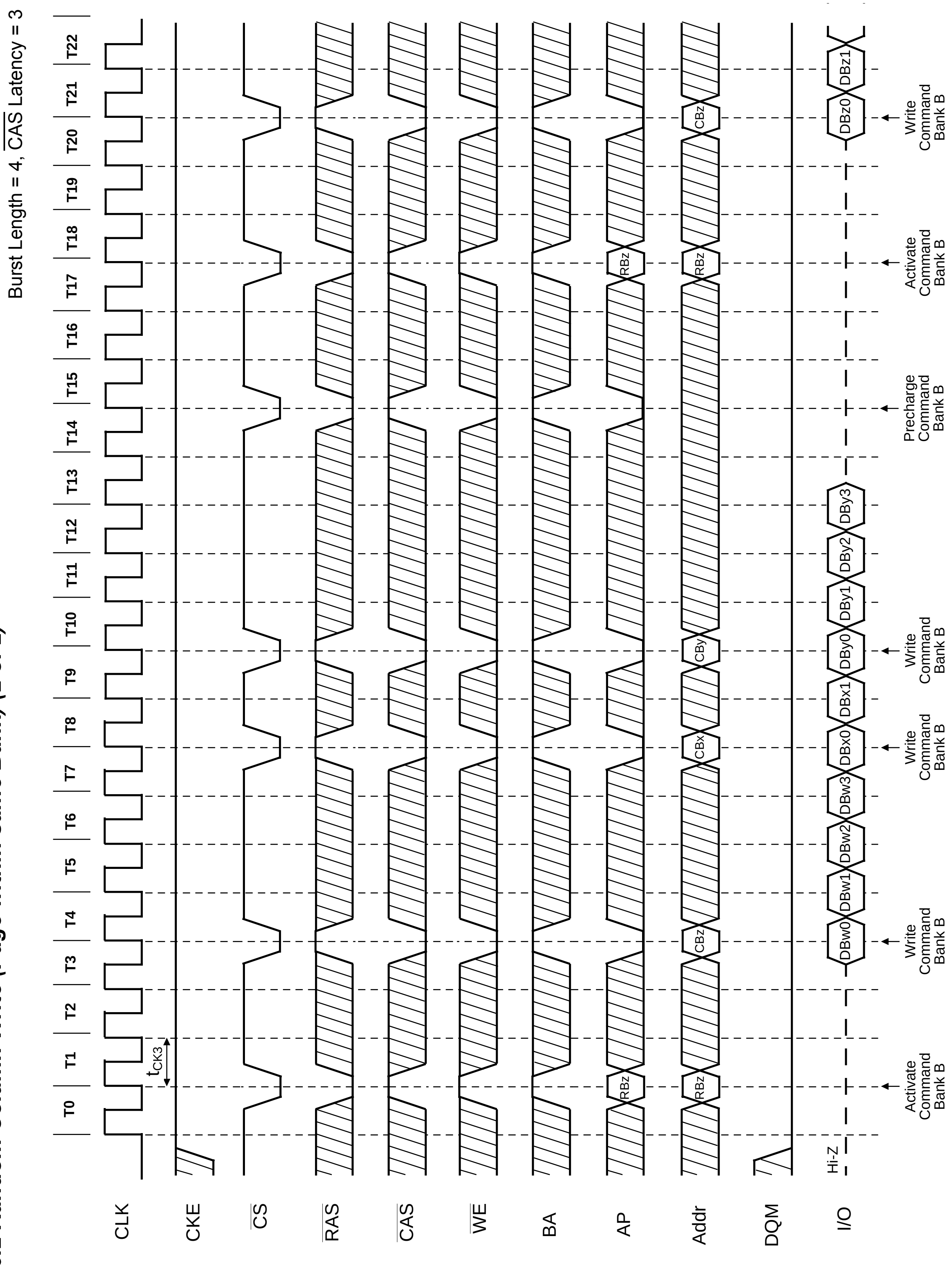


16.1 Random Column Write (Page within same Bank) (1 of 2)

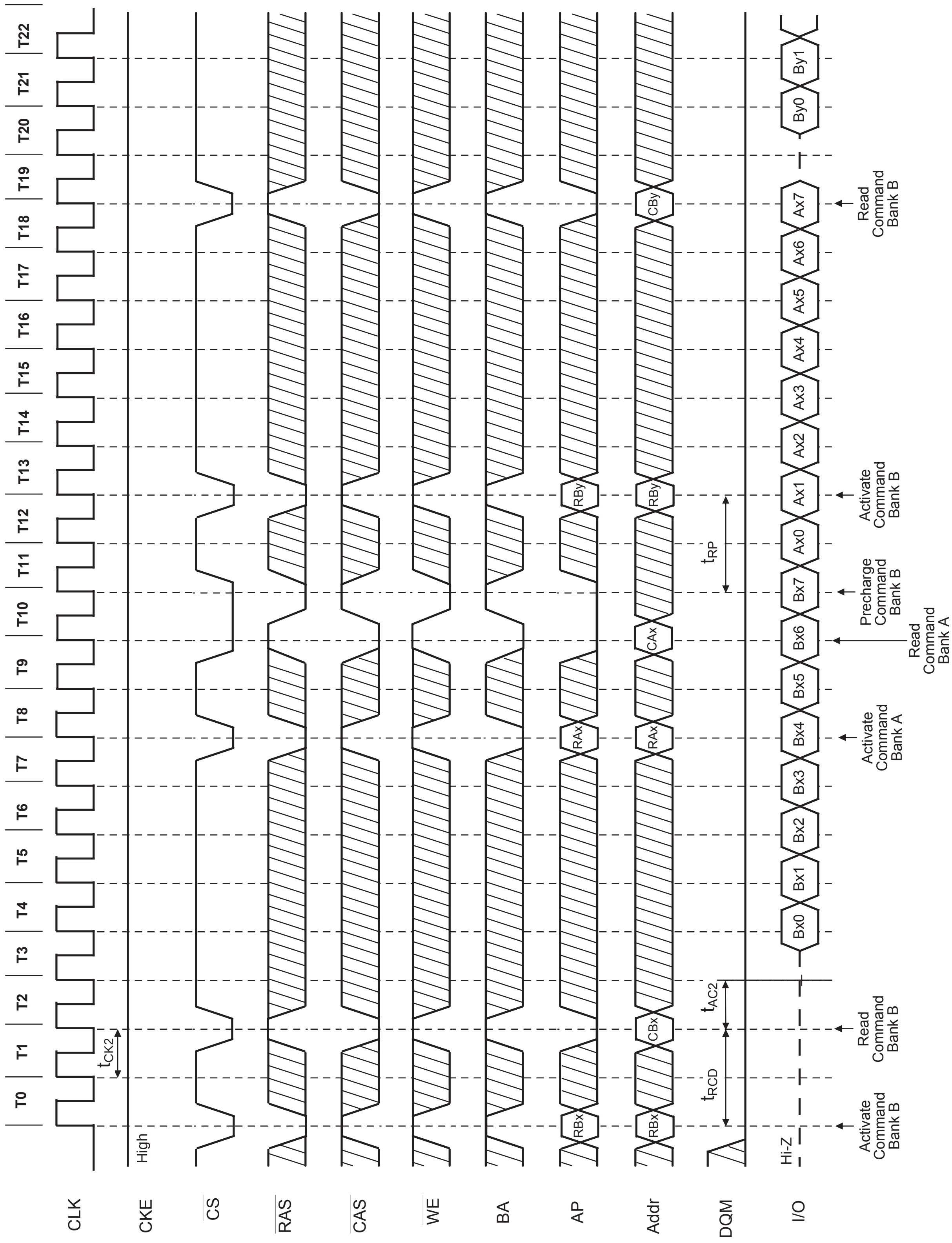
Burst Length = 4, $\overline{CAS}$ Latency = 2



16.2 Random Column Write (Page within same Bank) (2 of 2)

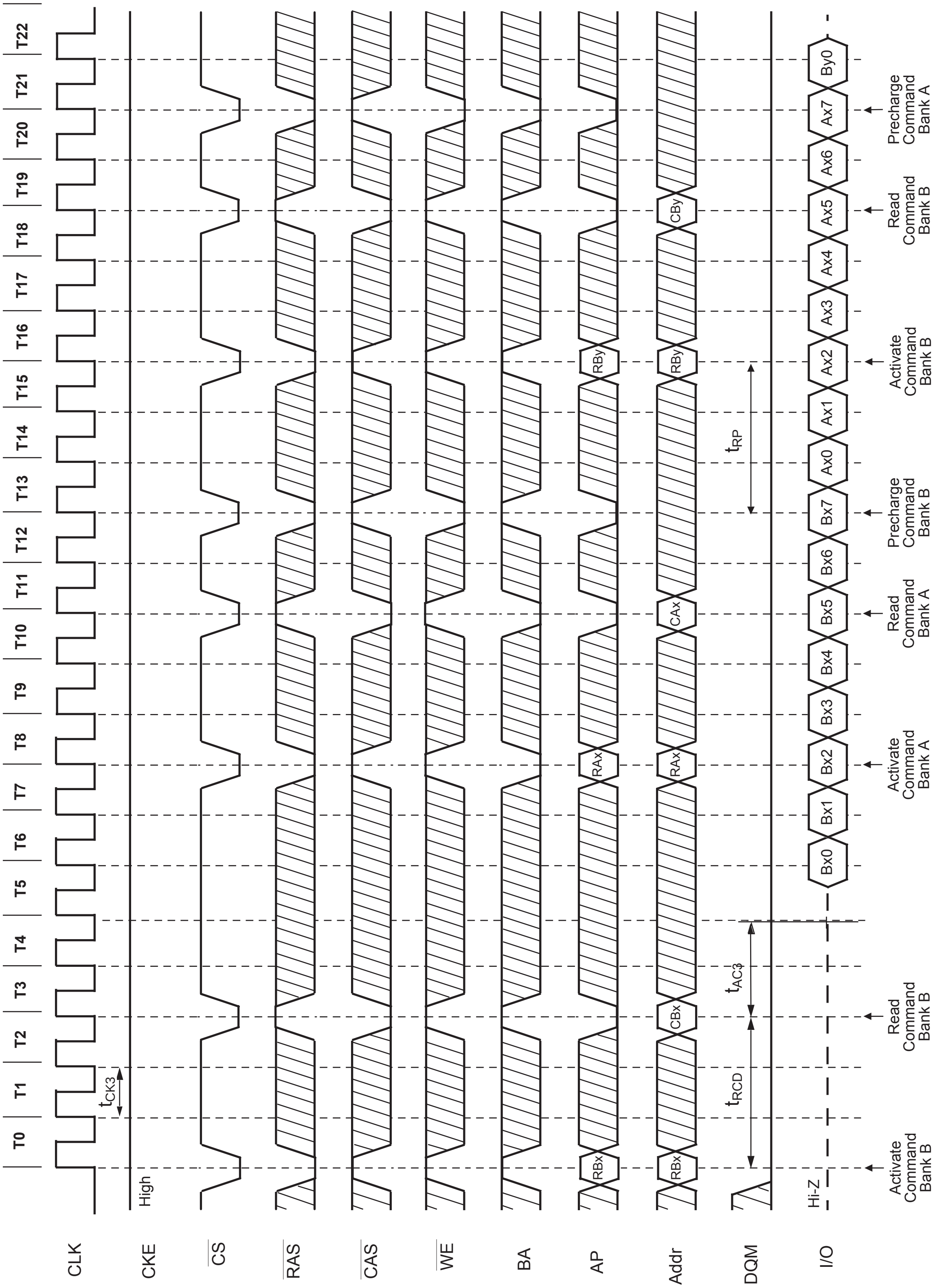


17.1 Random Row Read (Interleaving Banks) (1 of 2)



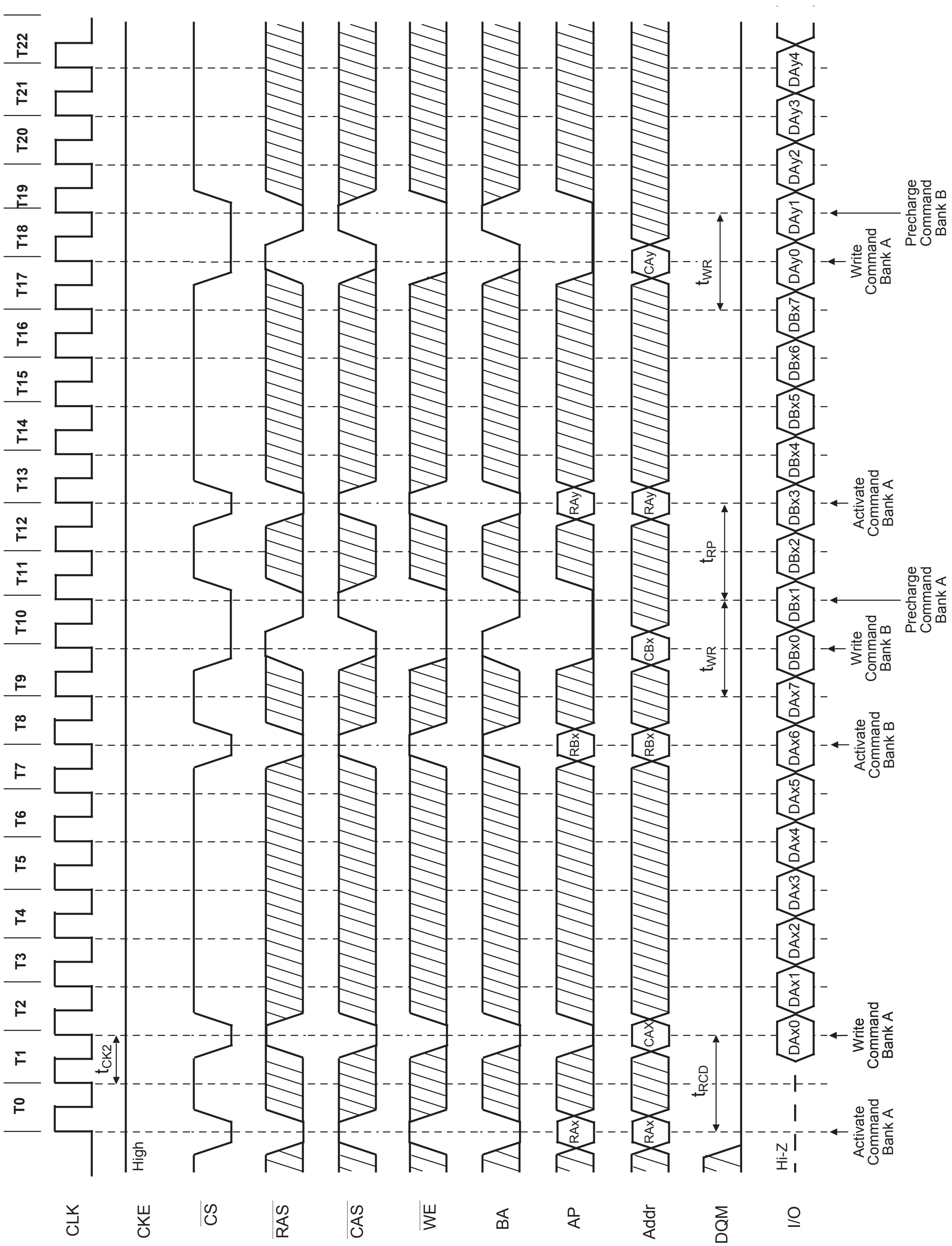
17. 2 Random Row Read (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3



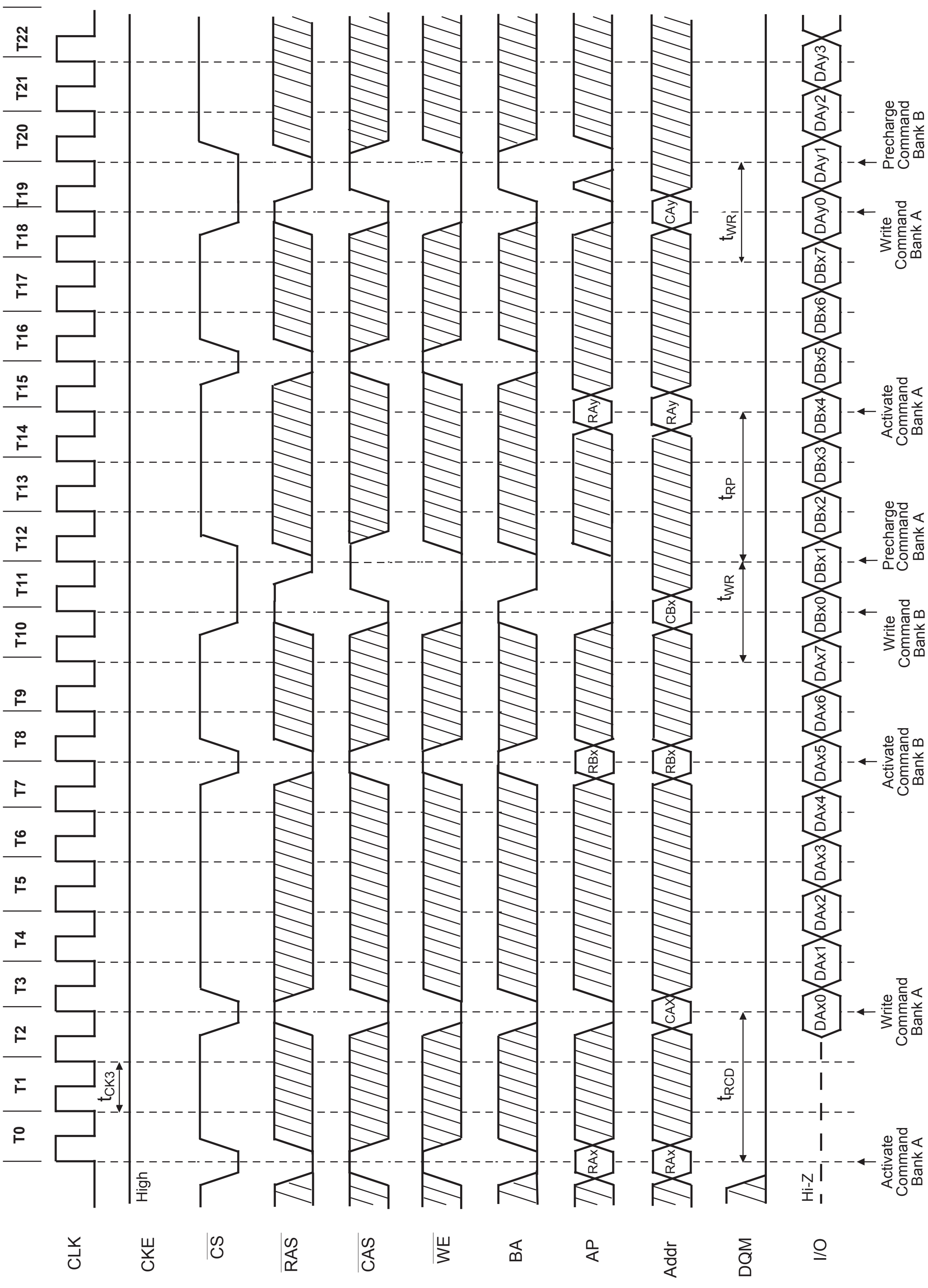
18.1 Random Row Write (Interleaving Banks) (1 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 2



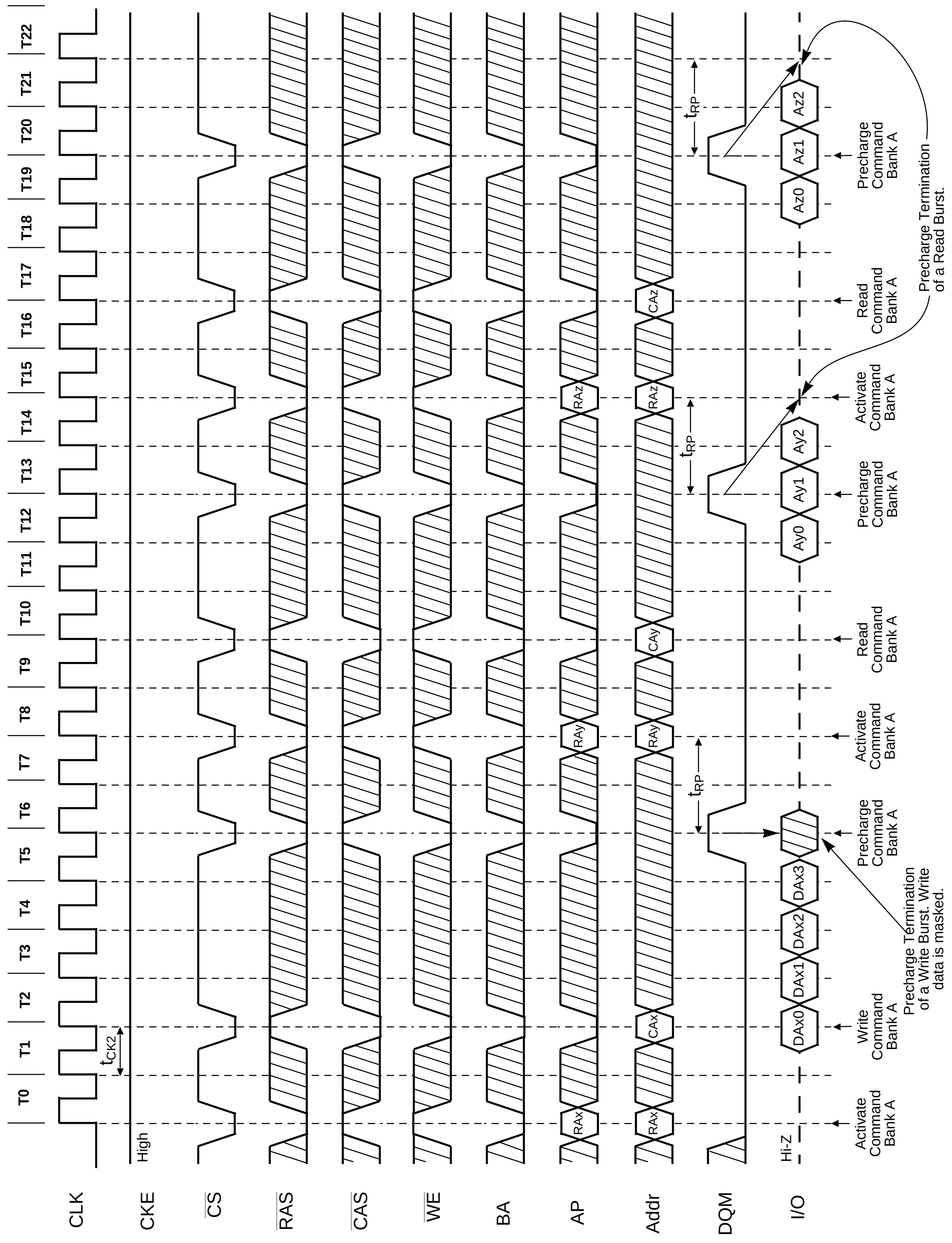
18.2 Random Row Write (Interleaving Banks) (2 of 2)

Burst Length = 8, $\overline{CAS}$ Latency = 3



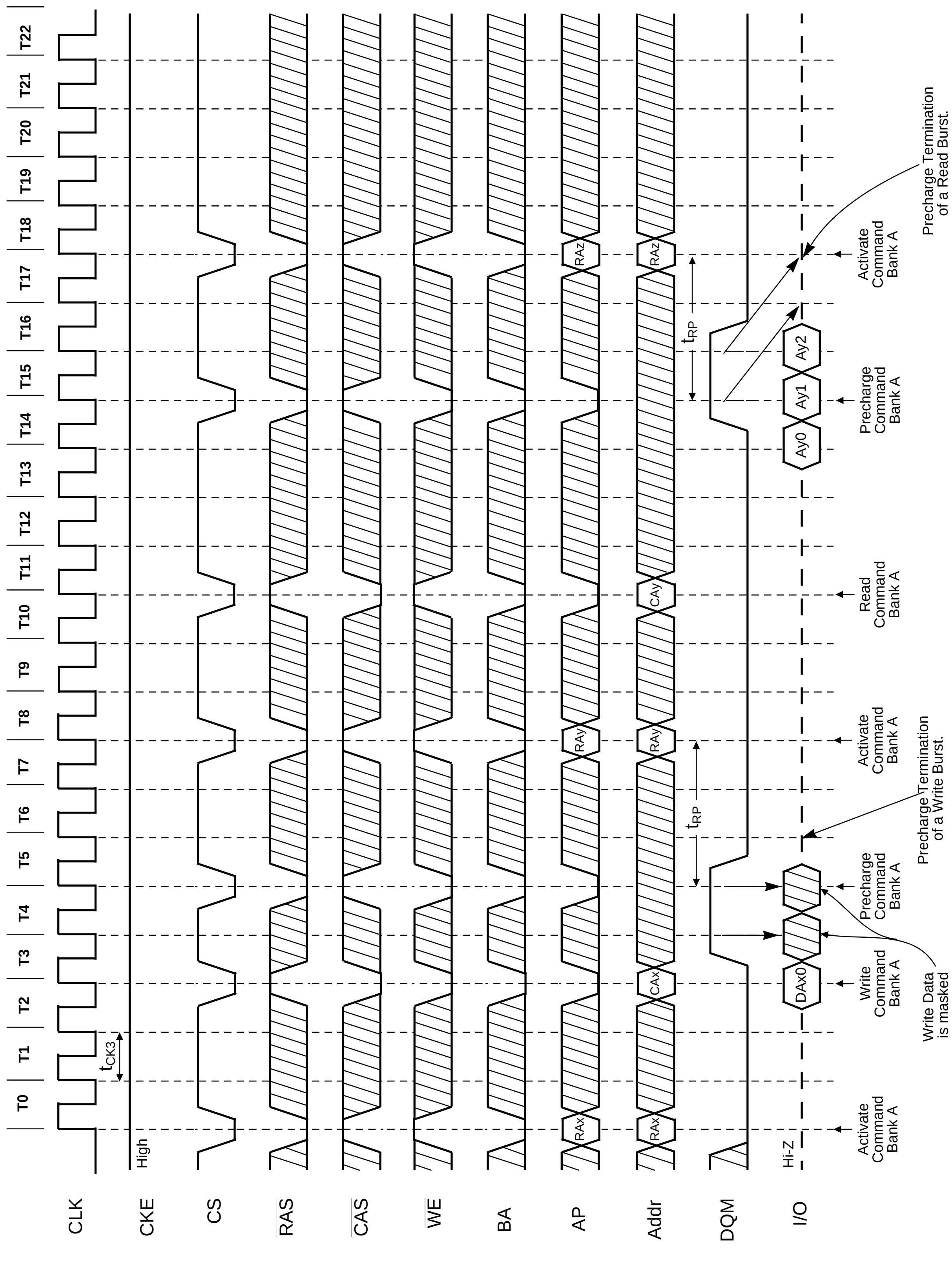
19.1 Precharge Termination of a Burst (1 of 2)

Burst Length = 8, CAS Latency = 2

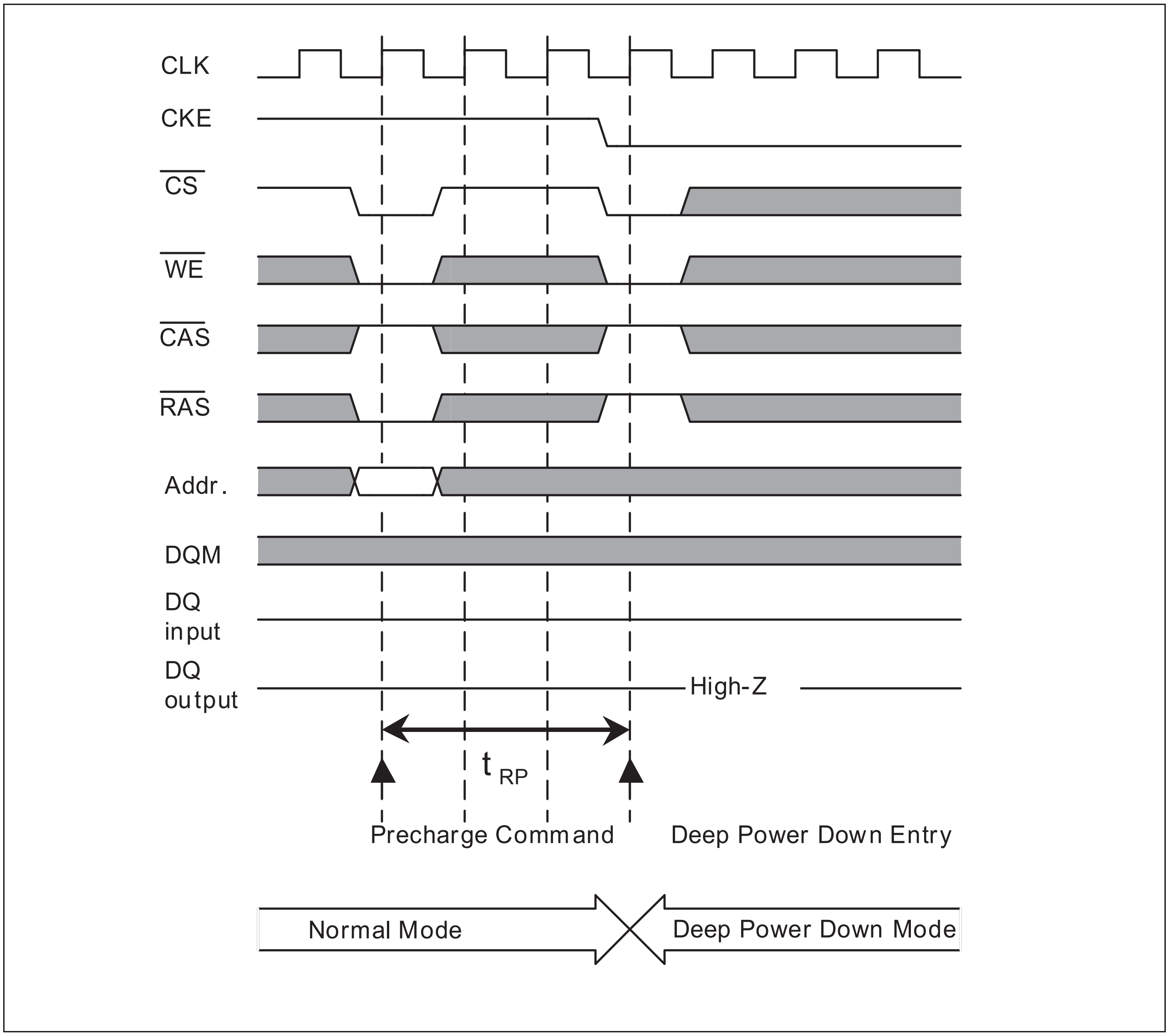


19.2 Precharge Termination of a Burst (2 of 2)

Burst Length = 4, 8, CAS Latency = 3



20.1 Deep Power Down Mode Entry

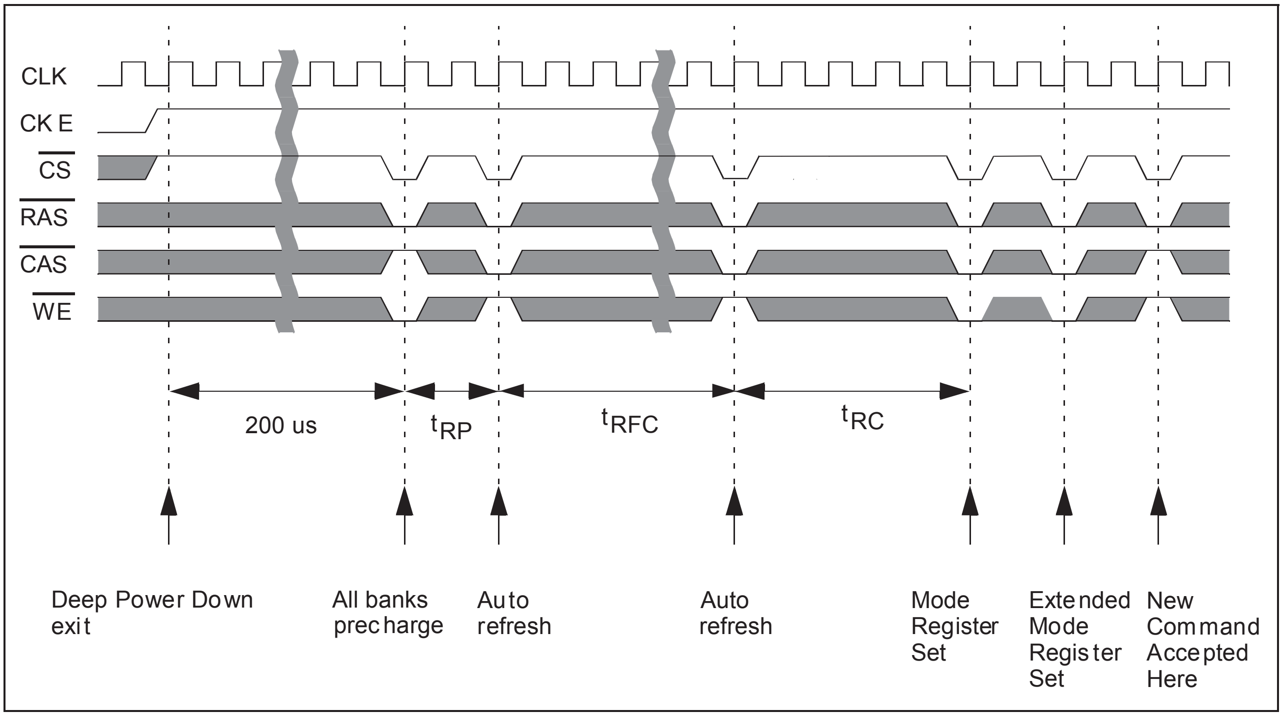


The deep power down mode has to be maintained for a minimum of 100µs

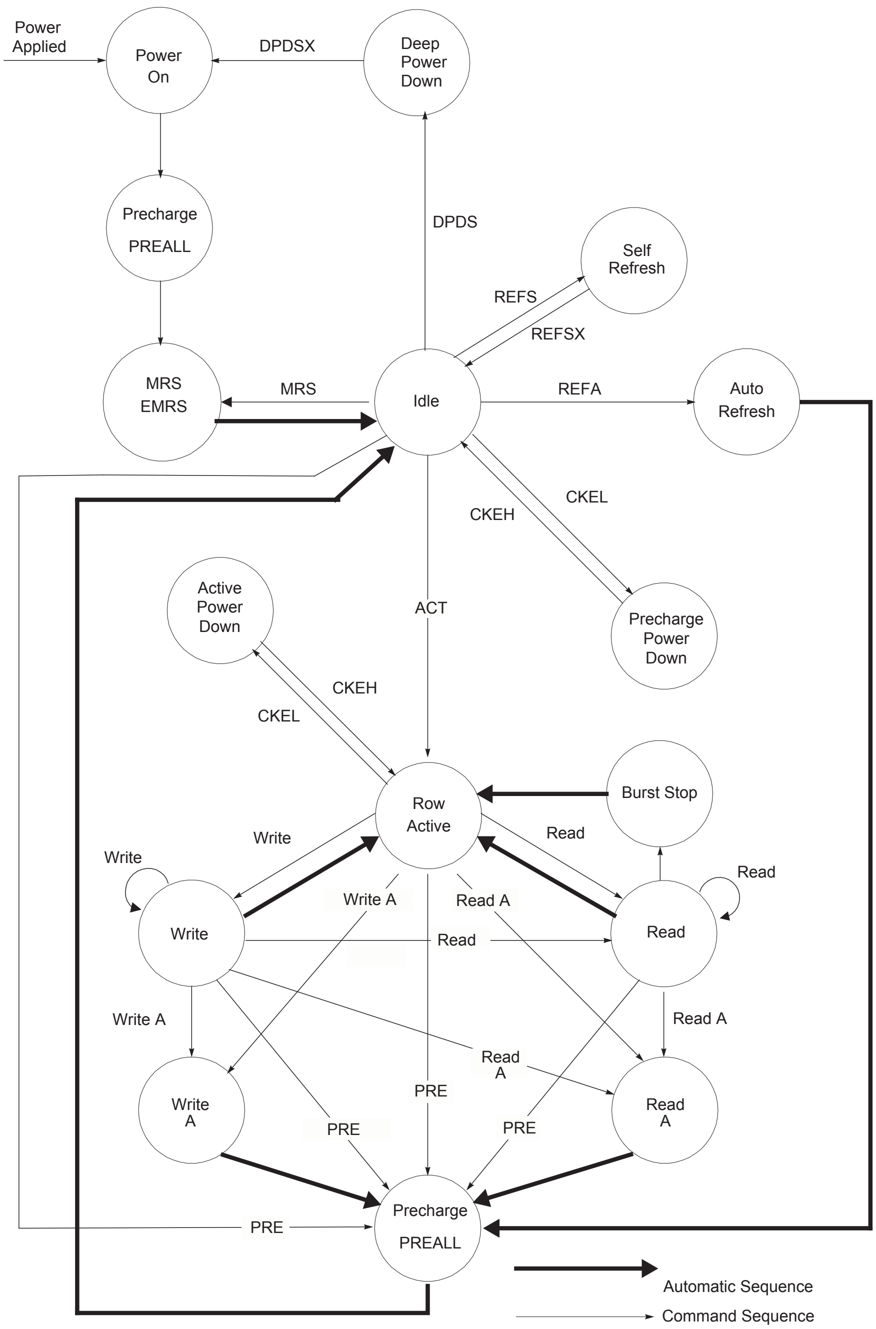
20.2 Deep Power Down Exit

The deep power down mode is exited by asserting CKE high. After the exit, the following sequence is needed to enter a new command:

1. Maintain NOP input conditions for a minimum of 200 µs
2. Issue precharge commands for all banks of the device
3. Issue eight or more autorefresh commands
4. Issue a mode register set command to initialize the mode register
5. Issue an extended mode register set command to initialize the extende mode register

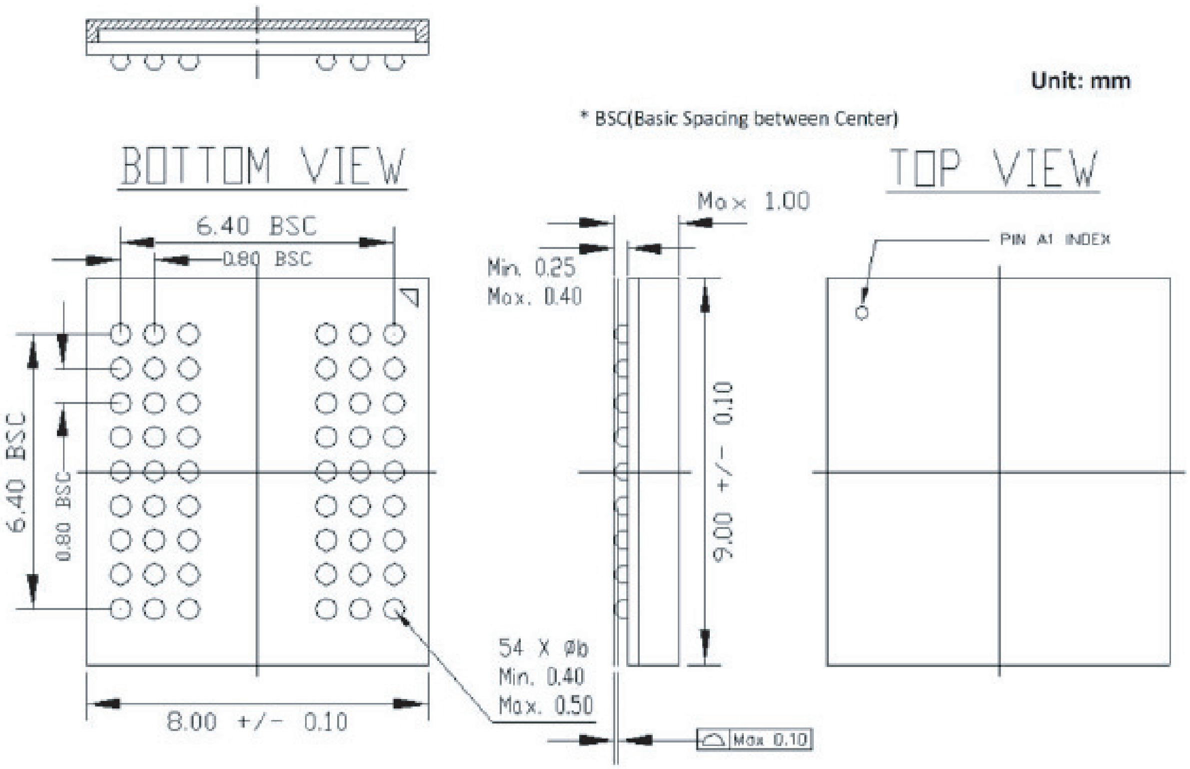


Mobile SDRAM State Diagram



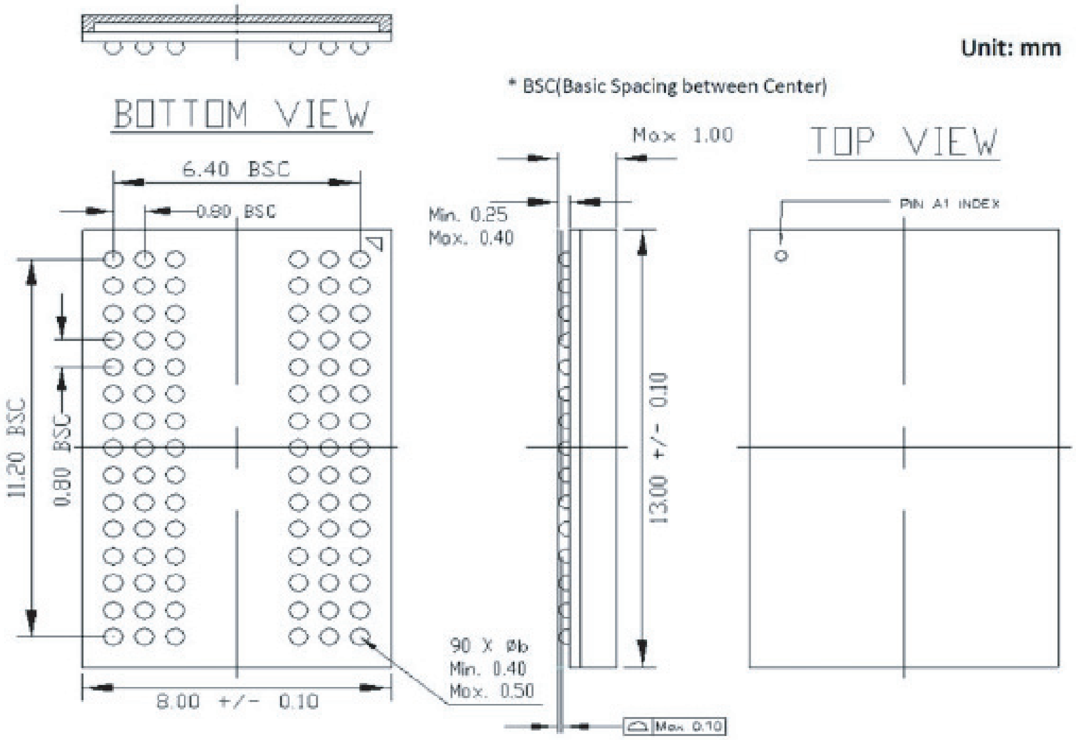
Package Diagram

32Mx16 54-BALL 0.8mm pitch BGA



Package Diagram

16Mx32 90-BALL 0.8mm pitch BGA



PART NUMBERING SYSTEM

AS4C	32M16MS or 16M32MS	6/7	B	C / I	N
DRAM	32M16=32Mx16 16M32=16Mx32 MS=Mobile SDRAM	6=166MHz 7=133MHz	B = FBGA	C=Commercial (-25° C~+85° C) I = Industrial (-40° C~+85° C)	Indicates Pb and Halogen Free

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